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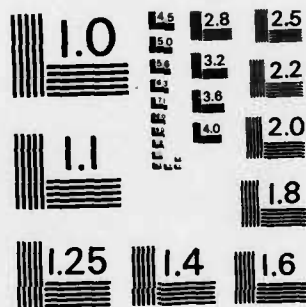
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Modulation Doped GaAs/Al_xGa_{1-x}As Layered Structures with Applications to Field Effect Transistors

Technical Report for the
Air Force Office of Scientific Research

for the Period
January, 1980 through December, 1982

by
Hadi Morkoc

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number) During this three year reporting period, we have established a device fabrication laboratory, dc and rf device testing facilities and materials characterization facilities. Initially, a great deal of effort was spent to improve the molecular beam epitaxial growth of heterojunctions. Later-on the dependence of heterojunction properties on the structural parameters were investigated in detail and in the process, separation of donor and electrons by about 200 Å in a modulation doped structure was discovered to		

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lead to extremely high electron mobilities.

Transport parallel to the heterointerface in normal and inverted structures was investigated at moderate fields for the first time. Polar optical phonon emission above 200 V/cm field strengths was found to be responsible for mobility reduction. High field transport properties was deduced from the FET performance. Since the ionized donors are located in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer, the GaAs layer having an interface sheet carrier concentration of about 10^{12}cm^{-2} is virtually free of ionized carriers. The high field transport parallel to the interface then becomes similar to pure GaAs crystal with peak electron velocities of about $2.1 \times 10^7\text{ cm/s}$ and $3.3 \times 10^7\text{ cm/s}$ at 300 and 77 K respectively. Compared to doped GaAs at comparable levels, these figures represent substantial improvements.

Modulation doped field effect transistors with a 1 μm gate length and a 3 μm channel length were fabricated and characterized under dc operating conditions at both 300 and 77 K. A model was also developed to analyze the device operation and performance. Using this model, the heterojunction structures were optimized ($\text{Al}_x\text{Ga}_{1-x}\text{As}$ doping level and the donor-electron separation) for high performance field effect transistors. Transconductances of as high as 275 mS/mm and over 400 mS/mm were obtained at 300 and 77 K respectively. Normally-off devices exhibited power gains of over 10 dB at 10 GHz. A simple prediction shows that these devices should exhibit switching speeds of about 10 ps and 5 ps at 300 and 77 K respectively in a digital circuit with fan out of 1, e.g. ring oscillators. Reported switching times in ring oscillators are about 17 and 12 ps at 300 and 77 K respectively which are about a factor 2 away from the expected performance.

In a different area, a scheme which replaces the Schottky barrier of a MESFET with a n^+/p^+ structures grown in situ with the channel layer was developed. Since the fabrication steps are identical to those of MESFETs with the exception of gate metal being ohmic, it is possible to obtain advantages sought in junction gate GaAs FETs. Devices with 1 μm gate lengths and 3 μm channel lengths exhibited large gate-drain breakdown voltages, transconductances of about 140 mS/mm and a maximum available gain of 10 dB at 9 GHz. In addition, by adjusting the parameters of the n^+/p^+ structure constant transconductances for linear amplifiers are possible.

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 MATTHEW J. KERPER
 Chief, Technical Information Division

LIST OF SYMBOLS

- E_i : Energy in the i^{th} subband
 \hbar : Reduced Planck's constant
 q : Electronic charge
 m^* : Effective mass in the conduction band
 δ_0 : Electric field perpendicular to the heterointerface in the triangular potential well
 i : Integer
 E_0 : 1st subband energy w.r.t. the bottom of the conduction band
 E_1 : 2nd subband energy
 ϵ_1 : Dielectric constant in GaAs
 $\bar{n}(x)$: Charge concentration in the triangular potential well
 δ_1 : Electric field (perpendicular to the heterointerface) at the interface in GaAs
 n_{so} : Equilibrium areal density of two dimensional electron gas
 γ_0 : Adjustable parameter relating E_0 to n_{so}
 γ_1 : Adjustable parameter relating E_1 to n_{so}
 D : Two dimensional density of states in the triangular potential well
 $V(d_1^+)$: Potential at the heterointerface when approached from the GaAs side
 k : Boltzmann constant
 T : Absolute temperature
 V : Potential depicting the conduction band edge w.r.t. the Fermi level
 $\rho(x)$: Charge density in the quasi space charge region of $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 ϵ_2 : Dielectric constant of $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 $N_{d^+}(x)$: Ionized donor concentration in $\text{Al}_x\text{Ga}_{1-x}\text{As}$

- $n(x)$: Electron concentration in the quasi space charge region
 N_d : Total donor concentration in $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 g : Degeneracy factor of the donor level in $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 E_d : Donor binding energy in $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 N_c : Density of states in the conduction band of $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 N'_d : Quantity equal to N_d/N_c
 g' : Quantity equal to $g \exp(E_d/kT)$
 $V(0)$: Potential at $x = 0$, boundary between the doped and undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 $\delta_2(-W_2)$: Electric field in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ at the edge of the depletion region
 W_2 : Distance from the doped-undoped boundary to the edge of the depletion region in $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 y : Quantity equaling $\exp \left[\frac{qV(-W_2)}{kT} \right]$
 $\delta_2(0)$: Electric field at the boundary between the doped and undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 $\epsilon_2(d_1^-)$: Electric field at the heterointerface in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 d_1 : Thickness of the undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer
 δ : Correction term arising from the degeneracy of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$
 (see Equation 25)
 ΔE_c : Conduction band edge energy discontinuity at the heterointerface
 $V(d_1^-)$: Potential at the heterointerface on the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ side
 E_{F1} : Fermi level at the heterointerface
 ΔE_{F0} : Asymptotic value of the Fermi level for very small 2DEG concentrations
 a : Slope of the Fermi level vs. 2DEG concentration for large concentrations
 Δd : Effective distance of the 2DEG from the heterointerface
 V_2 : Electrostatic potential across the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ if all of the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ were depleted

- d: Total thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ under the gate
- d_d : Thickness of the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ under the gate
- V_{p2} : The voltage necessary to deplete the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer
- ϕ_b : Barrier height of the Schottky gate
- V_G : Applied gate voltage
- V_{off} : Voltage necessary to deplete the 2DEG
- Q: Charge of the 2DEG
- $V_{\text{eff}}(x)$: Effective voltage along the channel modulating the 2DEG
- $V_c(x)$: Channel voltage under the gate
- I: Drain current
- Z: Width of device
- $v(x)$: Electron velocity
- μ : Electron mobility
- δ : Electric field parallel to the heterointerface in the potential well
- δ_c : Critical field above which velocity saturation occurs
- R_s : Source resistance
- V_D : Applied drain voltage
- V'_D : Intrinsic drain voltage
- R_D : Drain access resistance
- V'_G : Defined in equation (52)
- x: Distance from the source end of the gate towards the drain
- L: Gate length
- I_s : Drain saturation current
- β : Defined in equation (54)
- V_{s1} : Voltage in the channel under the gate at the onset of velocity saturation
- v_s : Saturation velocity

- g_m : Transconductance
 $g_m|_{\max}$: Maximum transconductance
 Q_T : Total charge under the gate
 V_{GS} : Gate-to-source voltage
 V_{GD} : Drain-to-gate voltage
 C_0 : Characteristic maximum capacitance under the gate
 C_{GS} : Gate-to-source capacitance
 C_{GD} : Gate-to-drain capacitance
 $(V_{po})_{2d}$: Electrostatic potential equilibrating the 2DEG $(d + \Delta d)$ away
 V_{20} : Electrostatic potential depleting the doped $Al_x Ga_{1-x} As$ to
 a depth equal to W_2

ABSTRACT

Lattice matched heterojunction structures have received a great deal of attention owing to their applications to high speed and optoelectronic devices. In designing devices with ultra small dimensions, it is necessary to obtain high carrier concentration in a controllable manner in a very narrow region of the epitaxial structure. Modulation doped $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ structures meet this requirement without degrading the quality of the semiconductor. This is done by doping the larger bandgap $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer quite heavily with donors. Electrons associated with donors in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer transfer to GaAs where they are confined in a quantum well about 100 Å wide at the heterointerface. Since the ionized donors are located in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer, the GaAs layer having an interface sheet carrier concentration of about 10^{12} cm^{-2} is virtually free of ionized carriers. The high field transport parallel to the interface then becomes similar to pure GaAs crystal with peak electron velocities of about $2.1 \times 10^7\text{ cm/s}$ and $3.3 \times 10^7\text{ cm/s}$ at 300 and 77 K respectively. Compared to doped GaAs at comparable levels, these figures represent substantial improvements.

Field effect transistors with a 1 μm gate length and a 3 μm channel length were fabricated and characterized under dc operating conditions at both 300 and 77 K. A model was also developed to analyze the device operation and performance. Using this model, the heterojunction structures were optimized ($\text{Al}_x\text{Ga}_{1-x}\text{As}$ doping level and the donor-electron separation) for high performance field effect transistors. Transconductances of as high as 275 mS/mm and over 400 mS/mm were obtained at 300 and 77 K respectively. Normally-off devices exhibited power gains of over 10 dB at 10 GHz. A simple prediction

shows that these devices should exhibit switching speeds of about 10 ps and 5 ps at 300 and 77 K respectively in a digital circuit with fan out of 1, e.g. ring oscillators. The experimental switching times obtained in ring oscillators are about 17 and 12 ps at 300 and 77 K respectively which are about a factor 2 away from the expected performance.

I. INTRODUCTION

The subject of high speed devices is a rather wide one and encompasses any device capable of operation above about 1 GHz. Depending on their use, these devices can be grouped into two categories, analog and digital devices. In general the analog devices are much faster than the digital ones and, needless to say, both types have different applications. This manuscript will be concerned with only the special high speed field effect transistors that can be best prepared by molecular beam epitaxy (MBE).

Devices intended for high speed applications need to have very short transit times between the input and the output. This can be obtained by choosing a semiconductor or a special structure which exhibits high carrier velocity and by reducing the distance that the carriers have to travel. In vertical devices e.g. bipolar junction transistors, the important distance is the base thickness. This means that the control of the base thickness is extremely important. Thicknesses below 1000 Å and extremely sharp doping profiles are needed and can best be obtained by molecular beam epitaxy.

Lateral three terminal devices, such as FETs, must have correspondingly small lateral dimensions. Small lateral dimensions also require small epitaxial layer thicknesses and larger doping. The drawback of very high carrier concentrations is that the electronic properties of the semiconductor degrade with increased doping. The point should be made very clear that for current conduction one needs electrons (preferred) or holes. In conventional structures, electrons and donors, and holes and acceptors are present in the same space. Using the heterojunction concept that can be

engineered by MBE it is possible to separate the electrons needed for current conduction from donors, minimizing their adverse effects.

Electrons associated with donors placed in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers of $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ heterojunction structures transfer to the GaAs layers. The resulting space charge sets up a strong electric field (over 10^5V/cm) at each interface and leads to the formation of a triangular potential well. Aided by the energy band gap discontinuity, the electrons are confined to the heterointerface and are spatially separated from the donors. This is a very convenient way of obtaining electron concentrations of over 10^{18}cm^{-3} essentially in a plane. Since the donors are separated from the electrons, the electron transport properties of undoped GaAs are preserved. This phenomenon is called modulation doping, the FET applications of which will be the main topic of this text.

In this chapter both the theoretical and experimental aspects of modulation doped field effect transistors (MODFETs) will be described. The interface sheet carrier concentration will be calculated in terms of both the triangular potential barrier, related energy levels and the device terminal voltages. Next, the drain saturation current will be calculated. This will be followed by the development of expressions for the transconductance and device capacitances. Following the device fabrication procedure, experimental and theoretical results as well as the effects of the dominant structural parameters will be discussed. Finally the high speed small signal and large signal results will be presented.

II. MODULATION DOPED FET

II. 1. MATERIALS CONSIDERATIONS

Modulation doped structures consist of single or multiple periods of doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) and undoped GaAs layer(s). The electrons transferring from the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer(s) into the undoped GaAs layer(s) are confined at the heterointerface as proposed by Esaki and Tsu in 1969 (1) and experimentally observed by Dingle et al in 1978 (2). Being spatially separated from the donors, the electrons, even at extremely high concentrations, are not subjected to ionized impurity scattering and thus can exhibit very high mobilities. This is especially pronounced at cryogenic temperatures where the ionized impurity scattering would have been dominant. The absence of ionized impurity scattering changes the dependence of mobility on lattice temperature in that it increases steadily as the temperature is decreased. In a perfect heterointerface the remaining scattering processes are the Coulombic interaction between the donors and electrons and the scattering due to background (in GaAs layers) ionized impurities. The results on MBE grown GaAs indicate that the total background ionized carrier concentration is in the high 10^{14} cm^{-3} range which should lower the low temperature mobility of modulation doped structures below about 50 K. The lack of such a drop in experimental mobilities is a result of high mobility electrons screening background ionized impurities very effectively. The details of such a screening mechanism have been treated by Price (3).

The Coulombic interaction between the donors and electrons across the heterointerface has also received a great deal of attention.

This interaction can be reduced by the incorporation of a thin undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer between the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer and the undoped GaAs layer. This concept was first introduced by the University of Illinois group (4,5,6) and adapted by every laboratory involved in this area of research. Using a spacer thickness of about 200 Å, electron mobilities of over $10^6 \text{ cm}^2/\text{Vs}$ at 4.2K have been obtained. Later on we will see that devices fabricated from structures exhibiting extremely high electron mobilities do not necessarily perform as well as those with thinner undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layers and, naturally, lower mobilities. As we will show in the following sections, the channel conductance of the modulation doped FETs is the parameter that should be optimized.

II. 2. STRUCTURAL PARAMETERS

We have so far briefly discussed the multiple period and single period structures but did not address the question of which one is better for FETs. Even though the multiple period structures are a means of producing many parallel paths and thus a large conductance these structures are not used for devices. This is a result of an asymmetry between the properties of GaAs grown prior to and after $\text{Al}_x\text{Ga}_{1-x}\text{As}$ growth. The heterointerface when the GaAs is grown on $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is not of high quality which makes the "inverted", and "multiple period" modulation doped structures unattractive (7,8). In this text then we will solely consider the normal single period structures where the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer is grown on an unintentionally doped GaAs buffer layer. It should, however, be remembered that a thin undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer still exists at the heterointerface.

The band diagram of a normal modulation doped structure is shown in Fig. 1 where the electrons confined at the interfacial triangular potential well have the characteristics of a two dimensional electron gas (9,10). In addition, higher order subbands formed in such a narrow ($\sim 50\text{\AA}$) quantum well may be populated if the electron concentration exceeds about high 10^{11}cm^{-2} . In such a case the electron mobility decreases, but improvements in the current carrying capability of the devices more than compensates for this reduction in mobility.

II. 3. MOBILITY AND VELOCITY CONSIDERATIONS

In many instances we have talked about electron mobility in the context of modulation doped FETs. In this section we will qualitatively relate the device performance to the mobility of carriers while keeping in mind that the electric fields present in short channel devices of this kind can be many times those where the mobility is no longer a constant with electric field. A schematic representation of such a surface oriented device (FET) having a gate length of $1\text{ }\mu\text{m}$ is shown in Fig. 2. For such short channel devices, the electric field is high, therefore the carrier velocity is the determining factor instead of the mobility. This text will treat the short channel FET with the understanding that the saturation velocity determines the FET performance. To do such a treatment we need to know the sheet carrier concentration at the heterointerface as well as its dependence on the gate voltage that is used to control it.

III. MODFET MODELLING

III. 1. INTERFACE SHEET CARRIER CONCENTRATION

To relate the sheet carrier concentration to energy levels, we must assume that the potential well at the heterointerface is triangular and that the electric field is quasi-constant. The solution of the longitudinal quantized energy is given by (11)

$$E_i = \left(\frac{\hbar^2}{2m^*} \right)^{1/3} \left(\frac{3}{2} n q \mathcal{E}_0 \right)^{2/3} \left(i + \frac{3}{4} \right)^{2/3} \quad (1)$$

where E_i is the energy, \mathcal{E}_0 the electric field at the interface and i an integer from 0 and up. The other parameters have their usual meanings. The energies of the two lowest subbands are thus

$$E_0 = 1.83 \times 10^{-6} \mathcal{E}_0^{2/3} \quad (2)$$

$$E_1 = 3.23 \times 10^{-6} \mathcal{E}_0^{2/3}$$

\mathcal{E}_0 in V/m

Experimental results should be used to modify the constants to minimize the adverse effects of the assumption that the electric field is constant.

The interface carrier concentration can be related to the sub-band energies if it is expressed in terms of the electric field. To do that Poisson's equation must be solved. In the depletion approximation and assuming no impurities in the GaAs layer (12)

$$\frac{d\mathcal{E}_0}{dx} = - \frac{q}{\epsilon_1} \bar{n}(x) \quad (3)$$

where $\bar{n}(x)$ and ϵ_1 , are the free electron concentration and the dielectric constant in the small bandgap material respectively.

Integration within the depletion region results in

$$\epsilon_1 = qn_{so} \quad (4)$$

where δ_1 and n_{so} are the interface electric field and carrier concentration respectively. Using equations (2) and (4)

$$E_o = \gamma_o (n_{so})^{2/3} \text{ and } E_1 = \gamma_1 (n_{so})^{2/3} \quad (5)$$

where γ_o and γ_1 , are adjustable parameters used to yield a good agreement with experiments.

Next we must establish a relationship between n_{so} and $qV(d_i^+)$.

E_F is taken as the reference energy so that the bottom of the conduction band $qV(d_i^+)$ represents the Fermi level (Fig. 3). The density of states associated with a single quantized energy level is given by (in $m^{-2}eV^{-1}$)

$$D = \frac{gm^*}{\pi\hbar^2} \quad (6)$$

and the interface carrier concentration can be calculated using the Fermi Dirac distribution (with a spin degeneracy of 2)

$$n_{so} = D \int_{E_0}^{E_1} \frac{dE}{1 + \exp\left(\frac{E - qV(d_1^+)}{kT}\right)} + 2D \int_{E_1}^{\infty} \frac{dE}{1 + \exp\left(\frac{E - qV(d_1^+)}{kT}\right)} \quad (7)$$

solving the integral (using $\int \frac{dx}{1+e^x} = \ln(1 + e^{-x})$) yields

$$n_{so} = DkT \ln \left[\left(1 + \exp\left(\frac{qV(d_1^+) - E_0}{kT}\right) \right) \left(1 + \exp\left(\frac{qV(d_1^+) - E_1}{kT}\right) \right) \right] \quad (8)$$

which for very low temperatures reduces to

$$n_{so} = D(qV(d_1^+) - E_0) \quad (9)$$

for an empty second subband or reduces to

$$n_{so} = D [qV(d_1^+) - E_0] + 2D [qV(d_1^+) - E_1] \quad (10)$$

for an occupied second subband. Using the experimental Shubnikov de Haas results (9) or cyclotron resonance measurements, the factors γ_0 and γ_1 can be estimated as

$$\begin{aligned} \gamma_0 &= 2.5 \times 10^{-12} (\text{J m}^{4/3}) \\ \gamma_1 &= 3.2 \times 10^{-12} (\text{J m}^{4/3}) \end{aligned} \quad (11)$$

and from the measured cyclotron mass

$$D = 3.24 \times 10^{17} (\text{m}^{-2} \text{ eV}^{-1}) \quad (12)$$

The interface sheet carrier concentration we just calculated must be provided by the larger bandgap semiconductor. Under equilibrium, the charge depleted from the larger bandgap material must equal the interface charge density. A solution is then found such that the Fermi level is constant across the heterointerface. Since the doping

level in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer is quite large (approaching the density of states), full depletion approximations can not be used (13). One must then use a charge which is a function of distance even with a constant doping. Therefore, the modified Poisson's equation is

$$\frac{d^2V}{dx^2} = \frac{-\rho(x)}{\epsilon_2} \quad (13)$$

Here, V is the electrostatic voltage and x is the perpendicular distance away from the heterointerface. The space charge density $\rho(x)$ is given by

$$\rho(x) = q [N_d^+(x) - n(x)] \quad (14)$$

where $n(x)$ is the free electron concentration and

$$N_d^+(x) = \frac{N_d}{1 + g \exp[(E_d + qV)/kT]} \quad (15)$$

is the ionized donor concentration. Here N_d is the total donor density, g is the degeneracy factor of the donor level and E_d is the donor activation energy. On the other hand (14)

$$n(x) = N_c \frac{e^{qV/kT}}{1 + \exp(qV/kT)/4} \quad (16)$$

where N_c is the density of states of the conduction band in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and the Fermi level E_F is chosen as the origin of the energy scale ($E_F=0$).

Combining equations (13) through (16), we obtain

$$\frac{d^2V}{dx^2} = -\frac{qN_c}{\epsilon_2} \frac{N'_d}{1 + g' \exp \frac{qV}{kT}} - \frac{\exp (qV/kT)}{1 + \exp (qV/kT)/4} \quad (17)$$

where $N'_d = \frac{N_d}{N_c}$ and $g' = g \exp (E_d/kT)$

The integration of equation (17) from $V(-W_2)$ to $V(0)$ with respect to V using the boundary condition $\delta_2(-W_2) = 0$ where δ_2 is the electric field in the $\text{Al}_{1-x}\text{Ga}_x\text{As}$ layer as shown in Fig. 3 and W_2 is the edge of the depletion region, yields

$$\begin{aligned} \delta_2^2(0) = \frac{2kTN_c}{\epsilon_2} \left[N'_d \ln \frac{g' + \exp \{-qV(0)/kT\}}{g' + \exp \{-qV(-W_2)/kT\}} \right. \\ \left. + 4 \ln \frac{4 + \exp \{qV(0)/kT\}}{4 + \exp \{qV(-W_2)/kT\}} \right] \quad (18) \end{aligned}$$

The constant $V(-W_2)$ can be found from the space charge neutrality that exists at $x = -W_2$, i.e.

$$\rho(-W_2) = -\frac{qN_c}{2} \left(\frac{N'_d}{1 + g' \exp \frac{qV(-W_2)}{kT}} - \frac{\exp \left(\frac{qV(-W_2)}{kT} \right)}{1 + \exp \left(\frac{qV(-W_2)}{kT} \right)/4} \right) \quad (19)$$

The solution of equation (19) is given by

$$y = \exp \frac{qV(-W_2)}{kT} = \frac{-\left(1 - \frac{N'_d}{4}\right) + \sqrt{\left(1 - \frac{N'_d}{4}\right)^2 + 4g'N'_d}}{2g'} \quad (20)$$

As can be seen from Figure 3, $V(-W_2)$ is simply equal to the difference between the Fermi level and the bottom of the conduction band edge away from the heterojunction. This value is shown in Fig. 4 as a function of the doping density at 300 and 77 K for the classical Boltzmann statistics or depletion approximation (solid line) and for the approximate Fermi-Dirac statistics (equation (19) dotted line). This comparison demonstrates that the deviation from Boltzmann statistics is quite noticeable even at a relatively low doping level, $N_d = 10^{17} \text{ cm}^{-3}$ and becomes quite substantial at doping densities commonly used ($1 - 2 \times 10^{18} \text{ cm}^{-3}$). The equilibrium interface density is determined by the interface field as

$$n_{so} = \frac{\epsilon_2}{q} \delta_2(0) = \frac{\epsilon_2}{q} \delta_2(d_1^-) \quad (21)$$

Equation (21) follows from Gauss' law if the doping density in the GaAs layer is small enough so that the total bulk charge in the depletion layer of GaAs is much smaller than qn_{so} . The expression for $\delta_2(0)$ is given by equation (18) which may be simplified when the inequality

$$\exp\left(-\frac{qV(0)}{kT}\right) \gg 1 \quad (22)$$

is taken into account, e.g.

$$\begin{aligned} \delta_2^2(0) = \frac{2qN_d}{\epsilon_2} \left\{ -V(0) + V(-W_2) - \frac{kT}{q} \left[\ln(1 + g'y) \right. \right. \\ \left. \left. + \frac{4}{N_d'} \ln\left(1 + \frac{y}{4}\right) \right] \right\} \quad (23) \end{aligned}$$

Substituting equation (23) into equation (21) yields

$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q} [-V(d_1^-) + V(-W_2) + \delta] + N_d^2 d_1^2} - N_d d_1 \quad (24)$$

where

$$\delta = -\frac{kT}{q} \left\{ \ln(1 + g'y) + \frac{4}{N_d'} \ln\left(1 + \frac{y}{4}\right) \right\} \quad (25)$$

The relationship

$$V(d_1^-) = V(0) - \phi_2(0) d_1 \quad (26)$$

has been incorporated to derive equation (24). The coordinate

$x = d_1^-$ corresponds to the $Al_xGa_{1-x}As$ side of the heterointerface.

Equation (24) differs from the depletion approximation case by δ in the right hand side which is subtracted from the total band bending

$$-V(d_1^-) + V(-W_2)$$

This contribution to the band bending is shown in Fig. 5 as a function of the doping density, N_d , in $Al_xGa_{1-x}As$ for 77 and 300 K. As can be seen from this figure the correction is quite important because it is comparable to ΔE_c .

In order to determine n_{so} , we should solve equation (24) with equation (8) which expresses n_{so} in terms of the density of states D and the two lowest energy levels in the potential well in GaAs as described earlier in equation (5).

Solving equations (24) and (8) simultaneously using (5), (25), (26) and

$$V(d_1^+) = \frac{1}{q} \Delta E_c + V(d_1^-) \quad (27)$$

with numerical techniques yields n_{so} , (dotted lines in Fig. 6). However, a very accurate analytical approximation can be obtained if equations (5) and (8) are linearized with respect to $V(d_1^+)$ as reported earlier (15,16). It should also be pointed out that $V(d_1^+)$ depicts the difference between the Fermi level (taken as reference) and the bottom of the conduction band in the GaAs at the heterointerface. It would be more appropriate to term $V(d_1^+)$ as E_{Fi}/q . Repeating equation with this replacement, we obtain

$$n_{so} = DkT \ln \left[\left(1 + \exp \left(\frac{E_{Fi} - E_o}{kT} \right) \right) \left(1 + \exp \left(\frac{E_{Fi} - E_1}{kT} \right) \right) \right] \quad (28)$$

With a little modification of equation (28), the linearization we discussed above can be realized. For large values of n_{so} we obtain

$$-\frac{1}{q} E_{Fi} = \frac{1}{q} \Delta E_{Fo}(T) + a n_{so} \quad (29)$$

where

$$a = 0.125 \times 10^{-16} (\text{V m}^{-2})$$

and $\Delta E_{Fo} = 0$ at 300 K and 25 meV at 77 K and below. Equation (28) leads to the following simple formula for n_{so} :

$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q} \left[\frac{\Delta E_c - \Delta E_{Fo}(T)}{q} + \delta + V(-W_2) \right] + N_d^2 (d_1 + \Delta d)^2 - N_d (d_1 + \Delta d)} \quad (30)$$

where

$$\Delta d = \frac{\epsilon_a}{q} \approx 80 \text{ \AA} \text{ (Ref. 15 and 16).}$$

If one were to use the depletion approximation in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer, the expression for the interface electron concentration can be arrived at by setting

$$\Delta E_c - \Delta E_{Fo}(T) = \delta = 0 \text{ in equation (30)}$$

$$n_{so} = \sqrt{\frac{2\epsilon_2 N_d}{q} [V(-W_2)] + N_d^2 (d_1 + \Delta d)^2} - N_d (d_1 + \Delta d). \quad (31)$$

Both at 77 K and 300 K, the depletion approximation underestimates the voltage term by 50 mV both at 300 K and 77 K, (see Fig. 5). In Fig. 8 the interface carrier concentration is plotted with respect to the thickness of the undoped interfacial layer. For comparison, experimental values obtained in our laboratory are also included (17). The large change in the measured n_{so} with respect to temperature not predicted by the theory is a result of the relatively thick doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer.

III. 2. CHARGE CONTROL

We have so far derived the expressions relating n_{so} to the parameters of the heterojunction structure. Since our intent is to fabricate and understand the operation of modulation doped FETs, we must derive the necessary expressions showing how n_{so} is modulated by the applied gate bias. A band diagram of such a heterojunction with a Schottky barrier (biased negatively) is shown in Fig. 9. As can be seen there are two depletion regions, one caused by the heterointerface and another by the Schottky barrier which will be referred to as the "gate". In the schematic diagram the doped $Al_xGa_{1-x}As$ layer is shown to be depleted entirely. This can be achieved by a combination of a sufficiently large gate voltage and/or a sufficiently thin doped $Al_xGa_{1-x}As$ layer.

Using equations (21) and (24), and assuming that the depletion approximation is accurate enough, we find

$$qn_{so} = \epsilon_2 \phi_2(0) = \sqrt{2q\epsilon_2 N_d \left[-V(d_1) + V(-W_2) \right] + q^2 N_d^2 d_1^2} - qN_d d_1 \quad (32)$$

which can then be used to calculate the electric field strength at the heterointerface. The same result can be obtained by the use of equation (23) in the light of depletion approximation.

Since the transport through $Al_xGa_{1-x}As$ is not as good as it is through GaAs, the structure and operational parameters are chosen such that the $Al_xGa_{1-x}As$ layer is depleted entirely. The electrostatic potential in such a case can be calculated simply by integrating the area

under the δ -field curve. One must, however, remember that the electric field is constant in the undoped spacer layer. If we assume that the thickness of the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is d_d , we find

$$V_2 = \frac{qN_d}{2\epsilon_2} d_d^2 - \delta_2(0)d \quad (33)$$

where $d = (d_d + d_i)$ and

$$\epsilon_2 \delta_2(d_i) = \epsilon_2 \delta_2(0) = qn_{so} = \frac{\epsilon_2}{d} (V_{p2} - V_2) \quad (34)$$

where

$$V_{p2} = \frac{qN_d}{2\epsilon_2} d_d^2 \quad (35)$$

is the voltage that is necessary to pinch off the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer. Examination of Fig. 9 shows that

$$V_2 = \phi_b - V_G + \frac{1}{q} (E_{F1} - \Delta E_c) \quad (36)$$

Combining equations (34) and (36) leads to

$$n_{so} = \frac{\epsilon_2}{qd} \left[V_G - (\phi_b - V_{p2} + \frac{1}{q} E_{F1} - \frac{1}{q} \Delta E_c) \right] \quad (37)$$

We must, however, remember that E_{F1} is a function of n_{so} as well as the gate voltage as depicted by equation (29). Substituting equation (29) into equation (37)

$$n_{so} = \frac{\epsilon_2}{qd} \left[V_G - (\phi_b - V_{p2} - \frac{1}{q} \Delta E_c + \frac{1}{q} \Delta E_{Fo}(T) + a n_{so}) \right] \quad (38)$$

or

$$n_{so} = \frac{\epsilon_2}{q(d + \Delta d)} (V_G - V_{off}) \quad (39)$$

where

$$V_{\text{off}} \equiv \phi_b - \frac{1}{q} \Delta E_c - V_{p2} + \frac{1}{q} \Delta E_{F0} \quad (40)$$

and

$$\Delta d = \frac{\epsilon_2^a}{q} \approx 80 \text{ \AA} \quad (41)$$

The charge is then given by

$$Q_s = qn_{so} = \frac{\epsilon_2}{(d + \Delta d)} (V_G - V_{\text{off}}) \quad (42)$$

If we were to assume that E_{F1} is not a function of the gate voltage, we would not have had the correction term $\Delta d (\approx 80 \text{ \AA})$ which can not be neglected next to d_d which is about 300 \AA . Thus Δd gives an important correction factor and dropping it can lead to overestimation of n_{so} for a particular V_G and thus to overestimation of current or underestimation of electron velocity.

III. 3. CURRENT CONTROL

In an FET configuration such as the one shown in Fig. 10, application of a drain voltage in addition to the gate voltage gives rise to a potential distribution varying from zero at the source end to V'_D at the drain (see Fig. 10). This potential then leads to an effective charge control voltage which is different from the applied gate voltage and is a function of distance under the gate. The potential distribution shown in Fig. 10 is obtained when the ohmic drop across the source and drain resistances are neglected. Later on we will incorporate these resistance, but for now the expressions and concepts become much simpler to understand without them.

At a distance x from the source, the effective voltage controlling the charge is

$$V_{\text{eff}}(x) = V_G - V_c(x) \quad (43)$$

where V_G and $V_c(x)$ are the external applied gate voltage, and the channel voltage respectively. Equation (42) must read

$$Q_s(x) = \frac{\epsilon_2}{(d + \Delta d)} [V_G - V_c(x) - V_{\text{off}}] \quad (44)$$

The channel current expression at x is

$$I = Q_s(x)Zv(x) \quad (45)$$

where Z denotes the width of the gate and $v(x)$ is the electron velocity at x . Since the gate dimensions we are concerned with are on the order of a $1 \mu\text{m}$ or less one must be concerned with high field effects such as velocity saturation.

We know that the electron mobility in the 2DEG is comparable to what is expected of pure GaAs (18). The electron saturation velocity also was reported to be what one can expect from a pure GaAs crystal without the degrading effects of ionized impurities. In this treatment we will use a two piece linear approximation (and briefly mention the three piece linear approximation) for the velocity field characteristic as shown in Fig. 11. Mathematically

$$v = \mu\delta \quad \text{for} \quad \delta < \delta_c \quad (46)$$

and

$$v = v_s \quad \text{for} \quad \delta \geq \delta_c \quad (47)$$

At fields less than δ_c , from equations (44) and (45), we obtain

$$I = \mu Z \frac{\epsilon_2}{d + \Delta d} \left[V_G - V_c(x) - V_{\text{off}} \right] \frac{dV_c}{dx} \quad (48)$$

where $dV_c/dx \equiv \delta$ is the electric field. As can be seen from Fig. 10, $\frac{dV_c}{dx}$ is maximum near the drain. For small drain voltages below saturation, one can assume that the linear region of the $v(\delta)$ curve is applicable.

For the case where $\delta < \delta_c$, integration of equation (48) with the use of

$$V_c(x=0) = R_s I \quad (49)$$

$$V'_D = V_c(x=L) = V_D - R_D I \quad (50)$$

where R_s and R_D denote the source and drain parasitic resistances and V_D depicts the external drain voltage, leads to

$$V_c(x) = V'_G - \sqrt{(V'_G - R_s I)^2 - 2 \frac{(d + \Delta d) I x}{\epsilon_2 \mu Z}} \quad (51)$$

where

$$V'_G = V_G - V_{off} \quad (52)$$

Differentiation of equation (51) with respect to x results in the electric field

$$\delta(x) = \frac{dV_c(x)}{dx} = \frac{(d + \Delta d)I}{\mu Z \epsilon_2} \left[(V'_G - R_s I)^2 - 2 \frac{(d + \Delta d)Ix}{\epsilon_2 \mu Z} \right]^{-\frac{1}{2}} \quad (53)$$

As we increase the drain voltage, the electric field near the drain end at $x = L$ will reach the critical value first, called ϵ_c or ϵ_s ;

$$\delta(x) \Big|_{x=L} = \delta_c = \left(\frac{I_s}{\beta L} \right) \left[(V'_G - R_s I_s)^2 - \frac{2I_s}{\beta} \right]^{-\frac{1}{2}} \quad (54)$$

where

$$\beta = \frac{\mu \epsilon_2 Z}{(d + \Delta d)L}$$

and I_s is the saturation current. Letting

$$V_{s1} = \delta_c L = \left(\frac{I_s}{\beta} \right) \left[(V'_G - R_s I_s)^2 - \frac{2I_s}{\beta} \right]^{-\frac{1}{2}} \quad (55)$$

then

$$\left(\frac{I_s}{\beta} \right)^2 \left[(V'_G - R_s I_s)^2 - \frac{2I_s}{\beta} \right]^{-1} - V_{s1}^2 = 0 \quad (56)$$

or

$$\left(\frac{I_s}{\beta} \right)^2 - V_{s1}^2 \left[(V'_G - R_s I_s)^2 - \frac{2I_s}{\beta} \right] = 0 \quad (57)$$

Solving for I_s leads to

$$I_s = \frac{\beta V_{s1}^2}{1 + (\beta R_s V'_G)^2} \left[\sqrt{1 + 2\beta R_s V'_G + (V'_G/V_{s1})^2} - (1 + \beta R_s V'_G) \right] \quad (58)$$

If R_s were to be set to 0, then

$$I_s = \beta v_{sl}^2 \left[\sqrt{1 + (v'_G/v_{sl})^2} - 1 \right] \quad (59)$$

or

$$I_s = \frac{\mu \epsilon_2 Z}{(d + \Delta d)L} \cdot v_{sl} \left[\sqrt{(v'_G)^2 + v_{sl}^2} - v_{sl} \right] \quad (60)$$

Using

$v_{sl} = \beta_c L$ and $\mu \beta_c = v_s$, one finds

$$I_s = \frac{Z \epsilon_2 v_s}{(d + \Delta d)} \left[\sqrt{(v'_G)^2 + v_{sl}^2} - v_{sl} \right] \quad (61)$$

From equation (51) with $R_s = 0$ and $x = L$

$$v_c(L) = v'_G - \sqrt{(v'_G)^2 - 2 \frac{I_s L (d + \Delta d)}{\mu \epsilon_2 Z}} \quad (62)$$

On the other hand

$$I_s = \frac{Z \epsilon_2 v_s}{(d + \Delta d)} (v'_G - v'_{DS}) \quad (63)$$

where v'_{DS} denotes the intrinsic drain to source voltage. Using equations (61) and (63), we find

$$v'_{DS} = v'_G + v_{sl} - \sqrt{(v'_G)^2 + v_{sl}^2} \quad (64)$$

Extrinsic drain to source voltage is then given by

$$v_{DS} = v'_G + v_{sl} - \sqrt{(v'_G)^2 + v_{sl}^2} + I_s (R_s + R_D) \quad (65)$$

III. 4. TRANSCONDUCTANCE

For short channel devices, V_{s1} can be small compared to V'_G and thus the expression for I_s can be reduced to

$$I_s = \frac{\epsilon_2 Z v_s}{d + \Delta d} V'_G \quad (66)$$

The intrinsic transconductance in the saturation regime is given by

$$\begin{aligned} g_m|_{\max} &= \left. \frac{\partial I_s}{\partial V'_G} \right|_{V_D} = \text{constant} \\ &= \frac{dI_s}{dV'_G} \cdot \frac{dV'_G}{dV_G} = \frac{\epsilon_2 Z v_s}{(d + \Delta d)} \cdot \frac{d}{dV_G} (V_G - V_{\text{off}}) \end{aligned} \quad (67)$$

$$g_m|_{\max} = \frac{\epsilon_2 Z v_s}{(d + \Delta d)} \quad (68)$$

For long channel devices, using equation (59),

$$g_m = \frac{\partial I_s}{\partial V'_G} = \beta \frac{V'_G}{\sqrt{1 + (V'_G/V_{s1})^2}} \quad (69)$$

$g_m|_{\max}$ is obtained at $V'_G|_{\max}$ which is the pinch-off voltage of the 2DEG

$$V'_G|_{\max} = V_{po}|_{2d} = \frac{q n_{so} (d + \Delta d)}{\epsilon_2} \quad (70)$$

Substituting equation (70) into equation (69) we obtain

$$g_m|_{\max} = \frac{q \mu Z n_{so}}{L} \left[1 + \left(\frac{q \mu n_{so} (d + \Delta d)}{\epsilon_2 v_s L} \right)^2 \right]^{-\frac{1}{2}} \quad (71)$$

which reduces to equation (68) for small values of L .

IV. SMALL SIGNAL GATE CAPACITANCE

In order to find the various device capacitances the total charge under the gate needs to be calculated. In the Shockley approximation the total charge is given by

$$Q_T = Z \int_0^L qn_{so} dx = Z \int_{V'_S}^{V'_D} qn_{so} \frac{dx}{dV_c} dV_c \quad (72)$$

Using equation (48), we find

$$I = Zq\mu n_{so} \frac{dV_c}{dx} = Z\mu \frac{\epsilon_2}{d+\Delta d} (V'_G - V_c) \frac{dV_c}{dx} \quad (73)$$

Integrating both sides of equation (73)

$$\int_0^L I dx = Z\mu \frac{\epsilon_2}{d+\Delta d} \int_{V'_S}^{V'_D} (V'_G - V_c) dV_c \quad (74)$$

which leads to

$$I = \frac{Z\mu}{L} \frac{\epsilon_2}{d+\Delta d} \cdot \frac{1}{2} [(V'_G - V'_S)^2 - (V'_G - V'_D)^2] \quad (75)$$

From equation (73)

$$\frac{dx}{dV_c} = \frac{Zq\mu n_{so}}{I} \quad (76)$$

Substituting equation (76) into equation (72) and using equation (75)

$$Q_T = Z \int_{V'_S}^{V'_D} \frac{Z\mu \left[\frac{\epsilon_2}{d+\Delta d} (V'_G - V_c) \right]^2}{\frac{Z\mu}{L} \frac{\epsilon_2}{d+\Delta d} \frac{1}{2} [(V'_{GS})^2 - (V'_{GD})^2]} dV_c \quad (77)$$

where $V'_{GS} = V'_G - V'_S$ and $V'_{GD} = V'_G - V'_D$

Then

$$Q_T = ZL \frac{\epsilon_2}{d+\Delta d} \frac{2}{(v'_{GS})^2 - (v'_{GD})^2} \int_{v'_S}^{v'_D} (v'_G - v_c)^2 dv_c$$

$$= \frac{2}{3} C_o \frac{(v'_{GS})^3 - (v'_{GD})^3}{(v'_{GS})^2 - (v'_{GD})^2} \quad (78)$$

where

$$C_o = \frac{\epsilon_2 ZL}{(d+\Delta d)} \quad (79)$$

$$C_{GS} = \frac{\partial Q_T}{\partial v'_{GS}} = \frac{2}{3} C_o \frac{v'_{GS}(v'_{GS} + 2 v'_{GD})}{(v'_{GS} + v'_{GD})^2} \quad (80)$$

and similarly the gate-drain capacitance is

$$C_{GD} = \frac{\partial Q}{\partial v'_{GD}} = \frac{2}{3} C_o \frac{v'_{GD}(v'_{GD} + 2 v'_{GS})}{(v'_{GS} + v'_{GD})^2} \quad (81)$$

In Fig. 12 and Fig. 13, the normalized capacitances C_{GS}/C_o and C_{GD}/C_o are plotted against the normalized drain-to-source voltage v'_{DS}/v_{s1} using the normalized gate voltage v'_{GS}/v_{s1} as the parameter. These capacitance values are calculated for the region below current saturation. Above saturation both capacitances should stay constant at about C_o . In addition, for sufficiently large voltages, e.g. 0.5 V, both C_{GS} and C_{GD} can be assumed constant having values of about $C_o/2$.

V. DEVICE FABRICATION

Shown in Fig. 14 is the schematic cross-sectional view of a single interface modulation doped field effect transistor (MODFET). Multiple interface MODFETs are not going to be covered here because of the asymmetry in the interface quality of GaAs on $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and $\text{Al}_x\text{Ga}_{1-x}\text{As}$ on GaAs (19,20). Inverted modulation doped structures with the binary on top of the ternary have also been fabricated (7) but their performance is still inferior because of a lower quality GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ interface (19).

Using the normal MODFETs with $\text{Al}_x\text{Ga}_{1-x}\text{As}$ on top of GaAs, the devices reported here were fabricated by first etching mesas which provide isolation of the devices and allows the gate contact pads to be placed on the Cr-doped semi-insulating substrate. The source and drain regions are then defined in positive photoresist and AuGe/Ni/Au metallization is evaporated. Following the lift-off process, this metallization is alloyed at 500°C for 1 minute in a H_2 ambient. The gate pattern is then defined with positive photoresist and the top $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer is thinned by etching, the amount of etching being dependent on whether a normally-off or a normally-on FET is desired, and the Al gate metallization is evaporated and lifted-off.

Figure 15 shows a top view of a MODFET having a gate length of $1\ \mu\text{m}$ and a source-drain spacing of $3\ \mu\text{m}$. The width of the device is $2 \times 145\ \mu\text{m}$. The source, drain and gate pads are built up to a total thickness of about $4000\ \text{\AA}$ to facilitate bonding. The wafer is then thinned down to about $200\ \mu\text{m}$ by polishing the back side. Following an electroless Pd plating process on the back side, the wafer is scribed and diced into individual devices. For dc testing the device

are first die bonded onto TO-18 headers and then wire bonded. For rf testing, the device is bonded to a microwave carrier and wire bonded to 50 Ω microstrip lines as shown in Fig. 16.

VI. COMPARISON OF THE THEORY WITH EXPERIMENTAL RESULTS

To test the accuracy of the model, a normally-off and a normally-on modulation doped FET fabricated in our lab were selected and characterized. The low field mobility was obtained from Van der Pauw-Hall measurements of the particular wafer from which the FETs were fabricated. The gate width is $145\text{ }\mu\text{m}$ and the length is $1\text{ }\mu\text{m}$. The structure consisted of a $1\text{ }\mu\text{m}$ undoped GaAs buffer layer, a $60\text{ }\text{\AA}$ undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer and a $600\text{ }\text{\AA}$ n-type $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer doped with Si to a level of $1 \times 10^{18}\text{ cm}^{-3}$. The $600\text{ }\text{\AA}$ dimension was used to allow fabrication of either normally-on or normally-off devices by recessing the gate. For $x = 0.3$, $N_d = 1 \times 10^{18}\text{ cm}^{-3}$ and $d_i = 60\text{ }\text{\AA}$, the doped (Al,Ga)As remaining beneath the gate should be about $250\text{ }\text{\AA}$ and $350\text{ }\text{\AA}$ thick to obtain normally-off and normally-on devices respectively.

The calculated and experimental drain saturation currents at room temperature as a function of the gate voltage are shown in Figures 17 and 18. $N_d = 1 \times 10^{18}\text{ cm}^{-3}$, $\mu = 6800\text{ cm}^2/\text{V}_s$ and $R_s = 7\Omega$ for the normally-on and 10Ω for the normally-off FETs were measured. $v_{\text{sat}} = 2 \times 10^7\text{ cm/sec}$ (18), $F_1 = 1\text{ kV/cm}$ and $F_2 = \mathcal{E}_c = 3.5\text{ kV/cm}$ are used for our calculation in Figures 17 and 18 (solid line: three piece velocity model; dotted line: two piece velocity model). The experimental values are marked by the dots. The measured transconductance of 275 mS/mm for the N-ON device at 300 K is the highest value ever reported. Even though 10Ω is measured as R_s for the N-OFF-FET, 12Ω is used for our model to have the best fit to the experimental data. A possible explanation for this is given below. As can be seen from Fig. 17, the agreement between our model and the experimental data is quite good except near the threshold (This region

is not described well by the model.)). The two piece model overestimates the current predicted by the three piece model by approximately 10-20%. The I_s-V_D characteristics for the N-on and N-off FETs are shown in Fig. 19 a) and b). As can be seen from the figure, the agreement between the measurement and our calculation is very good.

For the N-off FET, the agreement is also good but the value of R_s has to be adjusted to give a best fit. The slightly smaller current measured at $V_{GS} = 0.8$ V may be due to the fact that our model becomes invalid at gate voltage higher than $V_{off} + (V_{po})_{2d}$. The justification for using $R_s = 12\Omega$ instead of 10Ω may be as follows: The fabrication FET has $1 \mu m$ spacing between the source and gate. This region can be thought of as an ungated FET indicating that R_s should increase as the current increases. This effect should be more pronounced for N-OFF FET's

VII. EFFECT OF DONOR-ELECTRON SEPARATION

From equation (68) it is clear that any reduction in the thickness of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer under the gate leads to increased transconductances. This can either be done by increasing the doping in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (thereby reducing the thickness required under the gate) and/or reducing the undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer (21). Reduction of the spacer layer thickness also has the added advantage of leading to increased two dimensional electron concentrations. The resulting increased current carrying capability leads to a faster charging time of device and parasitic capacitances and thus to higher speeds. High speeds can be obtained at small voltage swings and thus low power consumption. This argument basically leads to the conclusion that the doping level in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer should be increased as much as possible and that the spacer layer should be made as small as possible.

The maximum net electron concentration that can be obtained in $\text{Al}_x\text{Ga}_{1-x}\text{As}$ doped with Si is about $2 \times 10^{18} \text{ cm}^{-3}$ which is smaller than Sn and Be doping limits possible by MBE. The limit in Si doping is thought to be a result of the high Si effusion cell temperature required. Any impurities present in the effusion cell assembly can easily be released at these high temperatures and incorporated in the growing $\text{Al}_x\text{Ga}_{1-x}\text{As}$ film. The Si doping limit in GaAs is about $5 \times 10^{18} \text{ cm}^{-3}$ which is basically comparable to the aforementioned figure for the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer. The use of a Si ribbon heated by passing current through it in place of an effusion cell has tentatively been shown to result in carrier concentrations of over 10^{19} cm^{-3} in GaAs (22).

Even if higher doping concentrations were possible, non-tunneling

Schottky barriers are difficult if not impossible to obtain on $\text{Al}_x\text{Ga}_{1-x}\text{As}$ with a doping level greater than about $2 \times 10^{18} \text{ cm}^{-3}$, which sets the practical limit.

The second parameter, the spacer layer, can be made as thick or as thin as one desires, meaning that there is no technological limit by the MBE process, except that a very thin layer may have to be incorporated to avoid Si diffusion into GaAs. Depending on the growth temperature, the required thickness to prevent Si atom diffusion for a conventional modulation doped FET structure is about $5\text{--}10 \text{ \AA}$. When the spacer layer is made this thin, the Coulomb interaction between the Si donors and the 2DEG is stronger which then may lead to a degradation of electron velocity. The electron velocity in undoped GaAs and doped (10^{17} cm^{-3}) GaAs layers is $1.8 \times 10^7 \text{ cm/s}$ and $2.1 \times 10^7 \text{ cm/s}$ respectively. This means that advantages gained in reducing spacer layer thickness must be weighed against the degradation in electron velocity. The experimental results obtained in our laboratory indicate that the optimum thickness is about 30 \AA .

To investigate the role of the undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer, a series of MODFET structures were grown and devices were fabricated (21) as described earlier. The doping level in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ was chosen to be about 10^{18} cm^{-3} so that adequate Schottky gates could be obtained.

As the thickness of the spacer layer was decreased from 100 \AA to 20 \AA a number of trends were observed. The decrease in the undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer thickness was closely matched by an increase in the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ thickness needed to accommodate the increased charge transfer. As a result, the gate capacitance remained almost constant while the maximum

saturation current almost doubled. On the other hand, the maximum transconductance scaled with current. The drain I-V characteristics of the best normally on and normally-off devices are shown in Fig. 20 indicating transconductances of 230 and 250 mS/mm respectively. The best previously reported values were 193 mS/mm for a normally-off device and 117 mS/mm (23) for a normally-on device. The maximum currents obtained are 12-20% higher than the best previously reported values. Recently optimized devices have shown improved current carrying capabilities up to twice those of the ones reported here.

The transistor characteristics were modeled using the equations derived earlier with the exact dependence of the Fermi level on the gate voltage accounted for. The saturation velocity was chosen to be 2×10^7 cm/s, independent of the mobility; on the basis of earlier work on modulation doped heterostructures (18). The two parameters used to fit the data were the doped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer thickness beneath the gate, d_1 , and the source resistance, R_s .

At 300 K, the mobility of the 2DEG is relatively independent of d_1 . Therefore we assume that $\mu = 7000 \text{ cm}^2/\text{Vs}$ and is independent of d_1 . The transconductance g_m vs. d_1 for a 1 μm gate devices is shown in Fig. 21 for the doping levels most commonly used. $N_d = 2 \times 10^{19} \text{ cm}^{-3}$ is also included (theoretical) to show the degree of dependence. It was pointed out earlier that non-tunneling Schottky barriers cannot be obtained at these doping levels. The dotted lines are obtained when Boltzmann statistics are used in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ and the solid lines take degeneracy into account.

Once the I_s vs. V_s characteristic was determined, the transconductance and gate capacitance were calculated numerically as $g_m = I_s/V_G$ and $C_g = dQ/dV_G$. While the values obtained for the transconductance are an accurate reflection of the experimental data, the capacitance values are good only as a first approximation.

Table I lists the source resistances used to model each device as well as the maximum saturation currents and transconductances. The data represent parameters for the largest value of I_s for which the data are accurately fit by the theory. These would be +0.6 V for the normally-off device and -0.2 V for the normally-on device in Figure 22 which shows the I_s vs. V_G characteristics of the best normally-on and normally-off devices fabricated. The maximum theoretical values of the saturation current and transconductance are given in parentheses.

The thicknesses of the undoped $Al_xGa_{1-x}As$ spacer, d_i , the doped $Al_xGa_{1-x}As$ beneath the gate, d_d , the equilibrium junction depletion depth, d_j , and the maximum gate capacitance are given in Table II. The large discrepancy in the parameter values of the 20 Å N-on FET relative to the other N-on devices results from it being only quasi-normally-on. The gate voltage swing ran from -0.4 V to +0.6. The current and transconductance values for this device are listed in Table II for $V_g = 0$ V. The normally-off device with $d_i = 20$ Å is anomalous in that the doped layer is too thin and the source resistance too small to be consistent with the other normally-off devices.

In Table II the gate capacitance is nearly independent of spacer layer thickness. This is a result of the particular parameters used rather than being a characteristic of MODFETs. The maximum capacitances tabulated represent an upper limit for devices operating a current saturation regime. This implies that maximum operating frequencies in excess of 10 GHz can be obtained.

VIII. CRYOGENIC TEMPERATURE PERFORMANCE

Conventional bulk GaAs layers doped to a level of 10^{17} cm^{-3} or higher do not show any appreciable mobility or velocity enhancement when cooled to 77K. Undoped GaAs, however, shows a considerable enhancement when cooled to 77K. This is a result of the absence of ionized impurities. Ironically, one must have ionized donors to obtain free electrons and thus current carrying capability. Modulation doped structures as described earlier provide electrons in sufficient numbers in the GaAs while maintaining its freedom from ionized impurities and, therefore, one would expect mobility-field and velocity-field characteristics similar to those of pure GaAs. Pulse measurements between 200 V/cm and 2kV/cm and dc measurements below 200 V/cm show that the transport in modulation doped structures is similar to that in pure GaAs (18). Static mobility-field and velocity-field characteristics of modulation doped structures along with undoped GaAs are shown in Figures 23 and 24 respectively.

Based on the above argument the transconductance of a short channel MODFET, being proportional to the electron velocity, should register an enhancement scaling with the velocity when cooled to 77K. For this experiment, the devices with an undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer thickness of 20 \AA were mounted on TO-18 headers and tested at 300K and, by immersing into LN_2 , at 77K. The drain I/V characteristics of a MODFET with a gate width of $290 \text{ }\mu\text{m}$ are shown in Fig. 25. For a gate voltage of +0.6V the transconductance is 225 mS/mm at 300K and 400 mS/mm at 77K. At $V_G = +0.8\text{V}$, the 2DEG is entirely depleted and an additional conduction path through the low quality $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is formed resulting in the observed decrease in transconductance.

Using the model described earlier the drain saturation current vs. gate voltage was calculated at 300 and 77K and plotted in Fig. 26. At 300K a source resistance of 4Ω and a saturation velocity of 2×10^7 cm/s were used. Such an excellent match in the entire range of currents can only be obtained for a specific combination of source resistance and saturation velocity making the values reported here very reliable. At 77K, R_s decreased to 2.5Ω and v_s increased to 3×10^7 cm/s. These results are in extremely good agreement with the predictions based on pulse measurements.

Also characterized in Fig. 26 is the best previously reported MODFET operating at 77 K (Fujitsu Laboratories, Ltd., Ref. 25). The data, represented as triangles, were taken from the published Fujitsu drain I-V characteristic. The dotted line is then calculated to fit the data. The Fujitsu device had a gate length of $2 \mu\text{m}$, a doping level of $N_d = 2 \times 10^{18} \text{ cm}^{-3}$ in the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and no undoped spacer layer. To model the device at 77 K the reported mobility of $20,000 \text{ cm}^2/\text{Vs}$ was used with $R_s = 3.8\Omega$ and $v_s = 3 \times 10^7 \text{ cm/s}$.

In all devices it is necessary to assume that 25% of the electrons in the $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ are frozen out at 77K to account for the shift in the threshold voltage. This figure was initially determined from measurements made on bulk $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ doped to $1 \times 10^{18} \text{ cm}^{-3}$ with Si. When modelling MODFETs, the thickness of the doped $\text{Al}_{0.33}\text{Ga}_{0.67}\text{As}$ beneath the gate is adjusted to result in a match between experimental and theoretical drain currents at a given gate voltage. At 300 K a thickness of 305 \AA was required to fit the data; at 77 K, assuming 25% freeze-out, the required thickness was 308 \AA . A consequence of the freeze-out is that the best parameters for a device intended for operation at cryogenic temperatures may not be the same as those optimizing the 300 K performance.

The transconductance of each device is calculated numerically from the curves in Fig. 26 ($g_m = \partial I_S / \partial V_G$) and plotted in Fig. 27. As can be seen, the potential maximum transconductance of our device at 77 K for a gate voltage of +0.8 V is 450 mS/mm at 77 K, as compared to a value of 400 mS/mm obtained for the Fujitsu device at 77 K. Calculating the maximum intrinsic transconductance (zero source resistance) for our device we find $g'_m = 352$ mS/mm at 300 K and 668 mS/mm at 77 K.

IX. HIGH FREQUENCY PERFORMANCE

For digital applications, inverters with an odd number of stages can be fabricated in a way to be connected in series. By bringing a feedback signal from the last stage to the first one, an oscillation, the frequency of which is a function of number of stages as well as the delay time associated with each device is obtained. In addition, parasitics such as line capacitances can add to the delay time. An output buffer stage, active or passive, is used to measure the oscillation frequency with a fast oscilloscope or a spectrum analyzer. Spectrum analyzers have the advantage that they can detect very weak signal levels.

The ring oscillators mentioned above have been fabricated and their performance has been reported (26,27). The best propagation delay time result obtained so far is 17 ps at 300 K with a power dissipation of slightly under 1 mW per gate with a gate length of 0.7 μm . At 77 K, the best performance is 12 ps with a power dissipation of about 10 mW per gate which must be trimmed down to about 1 mW to make refrigeration to 77 K practical (see Fig. 28).

High frequency small signal measurements made in our laboratory indicated a maximum available gain of about 12 dB at 10 GHz which compares well with published results by other laboratories (23). The noise measurements on individual devices (23) as well as cascaded three stage amplifiers have also been performed (28).

X. SUMMARY

Modulation doped $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ field effect transistors (MODFETs) whose operation is similar but performance is superior to Si/SiO_2 metal oxide semiconductor field effect transistors (MOSFETs) were described. A complete numerical model and very accurate analytical model with closed form expressions were developed and used to predict and improve the performance. The key aspect of the model is the use of the triangular potential well approximation to relate the two dimensional electron concentration (2DEG) to the subband energies. Using Gauss' law and Poisson's equation, the 2DEG is also related to the gate voltage as well as other hetero-junction parameters. The drain current of the MODFET was calculated using a two piece and also a three piece velocity-field model. From the charge under the gate the device capacitances were also calculated. Expressions for the transconductance were derived which indicate that, in terms of charge balance, the 2DEG can effectively be assumed to be 80 \AA away from heterointerface and if this correction is neglected it can lead to overestimation of current or underestimation of the electron velocity and also to overestimation of gate capacitance.

Devices with $1 \text{ }\mu\text{m}$ gate lengths showed extremely high transconductances and high current capabilities. The transconductances were observed to scale up with decreasing undoped spacer layer thickness. Maximum transconductances of about 275 mS/mm at 300 K and over 400 mS/mm at 77 K were obtained. By applying the model developed, the electron saturation velocity has been estimated to be $2 \times 10^7 \text{ cm/s}$ and $3 \times 10^7 \text{ cm/s}$ at 300 and 77 K respectively.

Microwave measurement on N-off MODFETs intended for logic circuit applications showed power gains of about 12 dB at 10 GHz . If

cooled to 77 K, better gains and very promising noise performance should be obtained. Ring oscillator data indicate switching speeds of about 17 and 12 ps at 300 and 77 K respectively.

Finally, improved fabrication techniques should lead to improved performance as well as applications to functional high speed integrated circuits. In a short time, switching times of 10 ps at 300 K should be possible. While the device itself should be capable of delivering an internal switching time of about 5 ps at 77 K, it may take a while to optimize the circuitry and device fabrication to deliver this expected performance.

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XI. APPENDIX A

In this section we will derive the expressions for the interface electric field and the sheet carrier concentration in the case where the depletion approximation is assumed applicable. Poisson's equation states

$$\frac{d^2 V_2}{dx^2} = - \frac{q}{\epsilon_2} N_2(x) \quad (A1)$$

where the parameters have their usual meanings and $N_2(x)$ is the donor concentration in the depletion region of the larger band gap material. Equation (A1) can be expressed in terms of the electric field. Referring to Fig. 3, we find

$$\frac{d\phi_2(x)}{dx} = \frac{q}{\epsilon_2} N_2(x) \quad (A2)$$

or

$$\frac{d\phi_2(x)}{dx} = \frac{q}{\epsilon_2} N_d \quad \text{for} \quad -W_2 < x < 0 \quad (A3)$$

where W_2 is the edge of depletion region. For $0 \leq x \leq d_1$

$$\frac{d\phi_2(x)}{dx} = 0 \quad (A4)$$

Solving equations (A3) and (A4) and using the boundary conditions that the electric field is continuous and is zero at $x = -W_2$, we obtain

$$\phi_2(x) = \frac{qN_d}{\epsilon_2} (x + W_2) \quad \text{for} \quad -W_2 < x < 0 \quad (A5)$$

and

$$\delta_2(x) = qN_d W_2 \quad \text{for } 0 \leq x < d_1 \quad (\text{A6})$$

These plots are shown in Fig. A1.

Integration of the electric field leads to the electrostatic voltage drop in the space charge region of the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer.

Starting with

$$V = -\int \mathcal{E} dx \quad (\text{A7})$$

we obtain

$$V_{20} = -\int_{d_1}^0 \frac{qN_d}{\epsilon_2} W_2 dx - \int_0^{-W_2} \frac{qN_d}{\epsilon_2} (x + W_2) dx \quad (\text{A8})$$

where $V_{20} = V(-W_2) - V(d_1^-)$. (See Fig. A2.)

From equation (A6),

$$\delta_2|_{d_1} = \delta_2(d_1^-) = \frac{qN_d W_2}{\epsilon_2} \quad (\text{A9})$$

and

$$\epsilon_2 \delta_2(d_1^-) = qN_d W_2 = qn_{so} \quad (\text{A10})$$

From equation (A8), the depletion depth can be found as

$$W_2^2 + 2W_2 d_1 - \frac{2\epsilon_2 V_{20}}{qN_d} = 0 \quad (\text{A11})$$

and thus

$$W_2 = -d_1 + \sqrt{d_1^2 + \frac{2\epsilon_2 V_{20}}{qN_d}} \quad (\text{A12})$$

Using equation (A10), and A(12), and noting $\phi_2(0) = \phi_2(d_i^-)$ one finds

$$\epsilon_2 \phi_2(d_i^-) = -qN_d d_i + \sqrt{q^2 N_d^2 d_i^2 + 2\epsilon_2 V_{20} q N_d} = qn_{so} \quad (A13)$$

This expression is identical to equation (32).

XII. APPENDIX B

ANALYSIS OF CAMEL GATE FETs (CAMFETs)

by

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ABSTRACT

The performance of camel gate GaAs FETs and its dependence on device parameters has been described. In particular, the dependence of the performance on the doping-thickness product of the p^+ layer was examined. Theoretical calculations indicate that using large p^+ doping-thickness products provides relatively voltage independent transconductances and large reverse breakdown voltages, both of which are desirable in large signal applications. Decreasing the p^+ doping increases the transconductance, which is desirable in logic applications. Comparison with performance of fabricated devices indicates good agreement between theory and experiment over a wide range of structural parameters. Microwave measurements on CAMFETs have yielded a gain of 10 dB at 9 GHz.

Introduction

The principle type of FET used at present for high frequency applications is the MESFET. This device uses a rectifying metal-semiconductor contact for modulating the width of the FET channel. The main virtue of this device is that the submicron dimensions required for high frequency operation are relatively easy to obtain. MESFETs, however, are beset with several problems. The metal-semiconductor contact tends to be unstable, particularly at high operating temperatures, leading to degraded reliability.²⁹ Further, the barrier height to current conduction is difficult to adjust. Schottky barriers with acceptable characteristics cannot be obtained on some small bandgap semiconductors such as InGaAs unless a tunneling oxide layer is used to enhance the barrier height.³⁰

An alternative to the MESFET is the JFET, which employs a p-n junction to modulate the channel. The p-n junction gate allows gate biases of up to +1V to be applied without appreciable gate conduction. However, these devices are relatively difficult to fabricate, particularly with the dimensions required for high frequency operation. In addition, they require that an ohmic contact be made to a p-type semiconductor, which can lead to large gate resistances.

An alternative to the JFET and MESFET has recently been proposed.³¹ The camel gate FET (CAMFET) uses very thin n^+ and p^+ layers, which together with the channel form a camel diode,³² to modulate the channel current. Use of the camel gate provides several advantages, including ease of fabrication, large barrier heights, and the potential for improved reliability and power handling capability.

Previously, some preliminary experimental results as well as the equations describing the camel gate FET have been presented.³¹ In this paper, the results of some theoretical calculations regarding the operation of the camel gate FET and their correlations with experimental results will be discussed.

Theoretical Performance

The basic structure of the camel gate FETs described here is illustrated in Figure B1, and the conduction band edge energy diagram of a homostructure device is illustrated in Figure B2. The structure consists of an undoped GaAs or (Al,Ga)As buffer layer, an n-type GaAs channel layer, a p⁺ GaAs or (Al,Ga)As layer, and an n⁺ GaAs layer. The parameters of the device are chosen so that the p⁺ layer is fully depleted in equilibrium. In the subsequent discussion, the device parameters are denoted as follows: N_d^+ , N_a , and N_d are the dopings of the n⁺, p⁺ and channel layers, respectively; t, d, and W denote the thickness of the p⁺ layer, and the depletion depths into the n⁺ and channel layers; and ϕ_B is the barrier height to current conduction via thermionic emission; and V_{n1} and V_{n2} denote positions of the Fermi level relative to the conduction band edge in the channel and n⁺ layers, respectively.

In order to understand how a camel gate FET operates, a theoretical description is useful. The describing equations of the camel gate FET are as follows. The channel depletion depth W satisfies

$$aW^2 + \beta W + \gamma = 0 \quad (B1)$$

where

$$\alpha = \frac{q}{2\epsilon_1} N_d \left(1 - \frac{N_d}{N_d^+} \right) \quad (B2)$$

$$\beta = \frac{qN_d t}{\epsilon_2} \left(1 + \frac{\epsilon_2}{\epsilon_1} \frac{N_a}{N_d^+} \right) \quad (B3)$$

$$\gamma = V_{n_2} - V_{n_1} + V_a - \frac{qN_a t^2}{2\epsilon_2} \left(1 + \frac{\epsilon_2}{\epsilon_1} \frac{N_a}{N_d^+} \right) \quad (B4)$$

and q is the electronic charge, ϵ_1 the dielectric constant of the n^+ and channel layers, ϵ_2 the dielectric constant of the p^+ layer, and V_a is the forward gate bias. The gate depletion capacitance C_{gs} , saturated velocity intrinsic transconductance s_m , barrier height ϕ_B , and depletion depth d are given respectively by

$$C_{gs} = \frac{A}{\frac{t}{\epsilon_2} \left(1 + \frac{\epsilon_2}{\epsilon_1} \frac{N_a}{N_d^+} \right) + \frac{W}{\epsilon_1} \left(1 - \frac{N_d}{N_d^+} \right)} \quad (B5)$$

$$s_m = \frac{v_s Z}{\frac{t}{\epsilon_2} \left(1 + \frac{\epsilon_2}{\epsilon_1} \frac{N_a}{N_d^+} \right) + \frac{W}{\epsilon_1} \left(1 - \frac{N_d}{N_d^+} \right)} \quad (B6)$$

$$\phi_B = \frac{qN_a}{2\epsilon_2} \left(t - \frac{WN_d}{N_d^+} \right)^2 + \frac{qN_d^+}{2\epsilon_1} \left[\frac{N_a}{N_d^+} \left(t - \frac{WN_d}{N_d^+} \right) \right]^2 \quad (B7)$$

and

$$d = t \frac{N_a}{N_d^+} - W \frac{N_d}{N_d^+} \quad (B8)$$

where A is the effective gate area, Z the effective gate length, v_s the electron saturation velocity, and ΔE_c the conduction band edge discontinuity at the p^+ -channel layer interface. In the following, the results of

calculations based on these equations will be presented. The values of the FET parameters used in the calculations were $N_d^+ = 7 \times 10^{18} \text{ cm}^{-3}$, $N_d = 2 \times 10^{17} \text{ cm}^{-3}$, and $t = 100 \text{ \AA}$, which are typical of actual devices. Since the doping-thickness product of the p^+ layer is most important in determining the performance of the device, the calculations were made for three different values of the p^+ layer doping N_a : 4×10^{18} , 7×10^{18} and $1 \times 10^{19} \text{ cm}^{-3}$. The p-layer semiconductor was assumed to be GaAs.

Figure B3 shows the barrier height ϕ_B as a function of gate reverse bias (i.e., gate negative with respect to the source). The barrier height is very sensitive to the p^+ doping level N_a , varying from a zero bias value of 1.2 V for $N_a = 1 \times 10^{19} \text{ cm}^{-3}$ down to 0.3 V for $N_a = 4 \times 10^{18} \text{ cm}^{-3}$. The barrier height may be increased by increasing the thickness and doping of the p^+ layer and decreasing the dopings of the n^+ and channel layers. In theory, the maximum barrier height possible is the semiconductor bandgap, the limit arising due to tunneling of electrons from the valence band in the p^+ layer to the conduction band of the n^+ layer. A larger bandgap material, such as (Al,Ga)As may be used to enhance the barrier height, although this has little effect on the potential depleting the channel.

An interesting feature of the barrier height in the camel gate FET is that it has a much stronger dependence on the gate voltage than does that of a Schottky barrier. Indeed, if the p^+ layer is lightly doped, the barrier height may be reduced to near zero with the application of a small reverse bias, leading to heavy gate conduction. By choosing the structural parameters properly, however, large barrier heights may be maintained for reverse gate biases in excess of 30 V.

The dependence of the depletion depth W into the FET channel on gate bias is illustrated in Figure B4. For comparison purposes, the depletion depth of a Schottky barrier with a 0.8 V built-in voltage is also illustrated. The depletion depth of a camel gate increases more slowly with applied bias than does that of a Schottky gate. This effect is related to the fact that the total charge in the depleted regions of the camel gate is fixed, and to the resulting reduction in barrier height with reverse bias.

Figure B5 gives the relation between d , the depletion depth into the n^+ layer, and the gate bias. The decrease in depletion depth with increasing reverse bias is a consequence of charge conservation. The sum of the charges in the n^+ and channel depletion layers is equal to the charge in the p^+ layer. Consequently, under reverse bias, an increase in the charge in the channel depletion layer must be accompanied by a corresponding decrease in that of the n^+ depletion layer. The depletion depth for $N_a = 1 \times 10^{19} \text{ cm}^{-3}$ is about 100 Å. For $N_d^+ = 7 \times 10^{18} \text{ cm}^{-3}$, surface states will deplete about another 120 Å, so that provided the n^+ layer thickness is less than about 200 Å, it will be fully depleted. As discussed later, this fact can greatly simplify the fabrication of the FET.

The intrinsic transconductance, g_m , of a CAMFET operating in the saturated velocity limit is illustrated in Figure B6. The saturation velocity was assumed to be $1.4 \times 10^7 \text{ cm/s}$. Again, the corresponding g_m for a MESFET with a 0.8 V barrier height is also indicated. By choosing a small p^+ doping, N_a , a large g_m can be obtained. Conversely, a large N_a yields a small g_m . Note also that for large N_a , g_m shows a relatively small variation with gate bias. Such a device should yield reduced third harmonic distortion and thus perform well as a linear amplifier.

The high frequency performance of an FET depends not only on the transconductance but on the gate capacitance C_{gs} , which is illustrated in Figure B7. It is important to note that, for short channel devices, the ratio g_m/C_{gs} depends only on geometrical factors and material parameters, and not on the structure of the layers. Consequently, the high frequency performance of camel gate FETs should be similar to that of MESFETs.

Experimental Performance

In order to investigate the properties of CAMFETs, a large number of devices with a wide range of parameters were fabricated. The layers from which these devices were fabricated were grown using molecular beam epitaxy on (100) Cr-doped semi-insulating substrates. The basic structure of the layers was given in Figure B1. The dopants used for the channel, p^+ and n^+ layers were Si, Be and Sn, with typical layer thicknesses of .2 μm , 100 \AA and 200 \AA , respectively. FETs were fabricated from the layers by first etching mesas and photolithographically defining the source and drain patterns. A AuGe/Ni/Au source and drain metallization was evaporated, lifted off, and alloyed into the FET channel at 400°C for 1 minute in an H_2 atmosphere. This procedure yielded contacts with specific contact resistivities in the low $10^{-6} \Omega \text{ cm}^{-2}$ range. The gate patterns were then defined and a Au gate metallization evaporated and lifted off. Alloying of the gate metal was not necessary because of the heavy doping of the n^+ GaAs layer. That the contacts were ohmic was verified experimentally, with good contacts being obtained for n^+ dopings as low as $4 \times 10^{18} \text{ cm}^{-3}$. The completed devices had a 3 μm source drain spacing, a 1 μm gate length, and a 145 μm gate width.

It is important to note that, other than the mesa etch, no etching is required in the fabrication of the CAMFET. In particular, etching of the n^+ and p^+ layers is not necessary because, as described earlier, for sufficiently thin n^+ layers, both the n^+ and p^+ layers are fully depleted and thus cannot contribute to conduction between the gate and source and drain.

As mentioned in the theory section, the doping-thickness product of the p^+ layer is most important in determining the properties of the camel gate. Thus several layers were grown with varying p^+ dopings and with the rest of the parameters similar. The parameters chosen were nominally $N_a^+ = 6 \times 10^{18} \text{ cm}^{-3}$, $N_d = 8 \times 10^{16} - 2 \times 10^{17} \text{ cm}^{-3}$ and $t = 100 \text{ \AA}$, and the n^+ layer thickness was 200 \AA . The p^+ doping was varied between $5 \times 10^{17} \text{ cm}^{-3}$ and $2 \times 10^{19} \text{ cm}^{-3}$.

Figure B8 shows the drain I-V characteristic of a CAMFET with $N_a = 3.5 \times 10^{18} \text{ cm}^{-3}$ and $N_d = 8 \times 10^{16} \text{ cm}^{-3}$, while Figure B9 shows the characteristic of a device with $N_a = 6 \times 10^{18}$ and $N_d = 1.5 \times 10^{17} \text{ cm}^{-3}$. Both devices had $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As } p^+$ layers. The transconductance of the device with the more heavily-doped p^+ -layer is smaller and varies less with gate bias than that of the more lightly doped device. This performance is consistent with the general trend that heavier p^+ doping leads to smaller, more uniform transconductances. These experimental results also agree with the theory.

Figures B10 and B11 give both the experimental and theoretical capacitance-voltage characteristics for FAIFETs fabricated on the same wafers as the devices in Figures B8 and B9, respectively, as well as experimental characteristics for Schottky-barrier FAIFETs with comparable channel dopings and identical geometries. The capacitance of the FAIFET of Figure B10, which has the more lightly doped p^+ layer, is quite comparable with that of the MESFET. The transconductances, forward gate-source I-V characteristics and

source resistances were also very similar. These results are consistent with the CAMFET's theoretical zero bias barrier height of 0.85 V. In contrast, the capacitance as well as transconductance of the camel FATFET with the more heavily doped p^+ -layer is smaller than that of the MESFET. The theoretical zero bias barrier height of this device was 1.35 V. Note the excellent agreement between theoretical and experimental capacitances in both figures.

The reverse gate-drain breakdown voltage was very sensitive to p^+ doping. For heavy p^+ dopings, as in the device of Figure B9, breakdown voltages of up to 30 V were obtained, compared with 10 V for MESFETs of similar geometry fabricated in our laboratory. Assuming a uniform channel field, for the given device geometry a 30 V breakdown voltage corresponds to a channel field of 300 kV/cm. This value is comparable to the breakdown voltage of bulk GaAs. In addition, the breakdown of the devices with heavily doped p^+ layers is very abrupt, characteristic of avalanche breakdown. As the p^+ doping was decreased, the breakdown voltage also decreased. For example, the device with a p^+ doping of $5 \times 10^{17} \text{ cm}^{-3}$ had a breakdown voltage of only 6 V. Further, breakdown of the more lightly doped devices tended to be quite "soft". These results again agree well with the theory, which predicts that for large p^+ dopings, appreciable barrier heights should be maintained even under large reverse bias. In this case, avalanching due to excessive fields should be the breakdown mechanism. On the other hand, smaller p^+ dopings should result in the barrier becoming very small at relatively small reverse gate biases. This barrier lowering gives rise to the current conduction at breakdown and the soft breakdown characteristics.

The implications of the experimental results presented above are that for power FETs, for which constant transconductances, large barrier heights, and

large breakdown voltages are desirable, the p^+ layer should be heavily doped. For logic applications, the speed is related to g_m/C_{gs} . Because parasitics can dominate the C_{gs} term, a large g_m and thus a smaller p^+ doping is indicated. Logic applications may also require larger barrier heights for compatibility with other circuits, and these may be obtained as well, although at the cost of reduced g_m .

Although larger p^+ doping-thickness products give larger barrier heights and more uniform g_m , eventually a product is reached for which the p^+ layer is no longer fully depleted. This results in shorting of the gate to the source and drain and necessitates etching of the n^+ and p^+ layers, which can be done by using the gate metal as a mask. The gate in this case consists of back-to-back diodes. Nevertheless, devices with good characteristics can still be obtained, as indicated in Figure B12.

In addition to varying the p^+ layer doping, the n^+ layer thickness was varied to determine the maximum thickness that would still be fully depleted. For a p^+ doping of $6 \times 10^{18} \text{ cm}^{-3}$ this thickness was found to be about 600 Å. Calculation of the depletion by the surface potential and by the p^+ layer, assuming a surface potential of 0.7 V and uniform doping profiles indicated an n^+ layer thickness of only 200 Å. The reason for the difference between these two values is not completely understood at this time, but may be due to surface segregation of the Sn in the n^+ layer.³³ This surface segregation could result in a nonuniform doping profile and thus in a larger depleted thickness than for a uniform profile.

An important factor in determining the commercial viability of the CAMFET is the ability to obtain the required control over layer dopings and thicknesses. For many applications, very uniform, controllable FET

characteristics over a large area are required. Clearly, the blessing of easy variation in CAMFET parameters with the p^+ layer doping-thickness product can become a curse if the dopings and thicknesses cannot be adequately controlled. Although a detailed analysis has not been performed, experimental results for MBE grown layers indicate the required doping profiles and in particular, p^+ layer charge, are obtained. And with current MBE technology, which employs rotating substrate holders, the uniformity requirements should be easily satisfied, making CAMFETs competitive with Schottky barrier FETs.

As a final note, microwave measurements on CAMFETs have been made. Figure B13 shows the maximum available gain (MAG) versus frequency characteristic for a device similar to that shown in Figure B8. The gain is approximately 10 dB at 9 GHz, and the cutoff frequency is about 30 GHz.

Conclusions

Based on the preceding discussion, camel gate FETs appear to have several virtues. Principle among these is the wide range of FET characteristics which may be obtained by varying the gate layer dopings and thicknesses. For given n^+ and channel layer dopings, a large p^+ doping-thickness product yields large gate-drain breakdown voltages and a relatively voltage independent transconductance, both of which are desirable in large signal applications. By using a small p^+ doping, larger transconductances, desirable in logic applications, may be obtained. Together with their ease of fabrication and potential for improved reliability, the advantages of camel gates should in future prove useful in a wide variety of applications.

XIII PUBLICATIONS UNDER THIS CONTRACT

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FIGURE CAPTIONS

- Fig. 1. Band diagram (drawn to scale) of a single period $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ modulation doped heterostructure having an undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ spacer layer thickness of 100 Å. The electron concentration in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is 10^{18} cm^{-3} .
- Fig. 2. A schematic representation of a cross-sectional view of a MODFET with the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ on top of the GaAs. Source and drain contacts are diffused in to reach the 2DEG plane. The gate metal (Al) is deposited after the channel has been recessed by chemical etching. The cap layer of GaAs is optional.
- Fig. 3. Conduction band edge diagram of a single period modulation doped heterostructure.
- Fig. 4. Conduction band edge energy in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ away from the hetero-interface with respect to the doping density for 300 and 77 K lattice temperatures.
- Fig. 5. The energy correction term arising from the degeneracy in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (without depletion approximation) as a function of the donor concentration in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer.
- Fig. 6. Interface sheet electron 2DEG concentration vs. the doping level in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer.
- Fig. 7. Interface Fermi potential (E_{F1}) vs. the sheet carrier concentration.
- Fig. 8. Interface sheet carrier concentration vs. the undoped spacer layer thickness.
- Fig. 9. Conduction band edge diagram of a single period modulation doped structure with a Schottky barrier deposited on the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer. Note that the $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer is shown to be depleted entirely by a combination of the Schottky gate and the space charge balancing the 2DEG.

- Fig. 10. Channel potential along the gate of a field effect transistor.
- Fig. 11. Assumed velocity vs. electric field characteristics, two piece and three piece models. The three piece model is for closely matching the cryogenic temperature velocity-field characteristic. Here F_2 corresponds to \mathcal{E}_c in the text.
- Fig. 12. The normalized gate-to-source capacitance vs. the normalized drain voltage.
- Fig. 13. The normalized gate-to-drain capacitance vs. the normalized drain voltage.
- Fig. 14. Cross-sectional view of a MODFET with a $.1\mu\text{m}$ gate length and a $3\mu\text{m}$ source-drain (channel) length.
- Fig. 15. Top view of a MODFET having dimensions indicated in the Fig. 14 caption.
- Fig. 16. Schematic diagram of a microwave carrier with 50Ω input and output microstrip lines used for rf measurements.
- Fig. 17. Drain saturation current (for a device width $Z = 145\mu\text{m}$) vs. gate voltage of a N-ON MODFET.
- Fig. 18. Drain saturation current (for a device with $(Z = 145\mu\text{m})$ vs. gate voltage of a N-OFF MODFET.
- Fig. 19. Three terminal output characteristics of the N-on and N-off MODFETs. Solid lines indicate the results of the three piece model, dots show measured data points and the broken lines show the two piece velocity-field characteristic result.
- Fig. 20. Output drain characteristics of a N-ON MODFET with $d_i = 40\text{ \AA}$ and a N-OFF MODFET with $d_i = 20\text{ \AA}$. Both characteristics are for $Z = 145\mu\text{m}$.

- Fig. 21. Intrinsic transconductance per mm of gate width given by $g_m/(1-g_m R_s)$ as a function of the undoped $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer thickness. Dotted lines assume non-degeneracy and solid lines assume degeneracy of doping in the $\text{Al}_x\text{Ga}_{1-x}\text{As}$. $V_{\text{off}} = 0.2 \text{ V}$, $\mu = 7,000 \text{ cm}^2/\text{Vs}$ and $L = 1 \text{ }\mu\text{m}$.
- Fig. 22. Saturation current vs. gate voltage characteristics for N-on and N-off MODFETs with $d_1 = 40 \text{ }\text{\AA}$. The measured data are presented as open circles ($Z = 145 \text{ }\mu\text{m}$).
- Fig. 23. Static electron mobility vs. electric field in a modulation doped GaAs/ $\text{Al}_x\text{Ga}_{1-x}\text{As}$ heterostructures deduced from pulse measurements up to an electric field of 2 kV/cm . Monte Carlo calculation up to 6 kV/cm are also shown for comparison for pure GaAs and GaAs doped to 10^{17} cm^{-3} .
- Fig. 24. Drift velocity vs. electric field in a modulation doped heterostructure up to an electric field of 300 V/cm . GaAs with an ion concentrations of 10^{15} and 10^{17} cm^{-3} is also shown (Monte Carlo calculations).
- Fig. 25. Drain I/V characteristics of a modulation doped FET having gate dimensions of $1 \text{ }\mu\text{m} \times 290 \text{ }\mu\text{m}$ at 300 K (a) and 77 K (b).
- Fig. 26. Drain saturation as a function of gate voltage of the device shown in Fig. 25. For comparison, the saturation current of a high performance Fujitsu device is also shown.
- Fig. 27. Calculated transconductance as a function of gate voltage using drain current vs. gate voltage characteristics shown in Fig. 26.

Fig. 28. Propagation delay vs. power consumption chart obtained from ring oscillators made from devices competing for high speed including the MODFETs.

Fig. A1. Electric field vs. distance, x , in the space charge region.

Fig. A2. Potential vs. distance in the space charge region.

Fig. B1. Schematic cross-section of a camel gate FET.

Fig. B2. Conduction band edge energy diagram of a homostructure camel gate FET. The shading denotes the depletion regions in the n^+ , p^+ and n layers.

Fig. B3. Barrier height to current conduction via thermionic emission ϕ_B vs. gate reverse bias.

Fig. B4. Depletion depth W into the FET channel vs. gate reverse bias. The depletion depth for a .8 V Schottky barrier gate is also indicated.

Fig. B5. Depletion depth d into the n^+ layer vs. gate reverse bias.

Fig. B6. Intrinsic transconductance of a CAMFET operating in the saturated velocity limit vs. gate reverse bias, as well as that of a Schottky gate FET.

Fig. B7. Gate capacitance per unit area vs. gate reverse bias.

Fig. B8. Drain I-V characteristic of a CAMFET with $N_a = 3.5 \times 10^{18} \text{ cm}^{-3}$ and $N_d = 8 \times 10^{16} \text{ cm}^{-3}$.

Fig. B9. Drain I-V characteristic of a CAMFET with $N_a = 6 \times 10^{18} \text{ cm}^{-3}$ and $N_d = 1.5 \times 10^{17} \text{ cm}^{-3}$.

Fig. B10. Experimental and theoretical gate capacitances for a FATFET fabricated on the same wafer as the device of Figure 8, as well as the experimental gate capacitance of a Schottky barrier FATFET with identical geometry and similar channel doping. The FATFET area is $4.6 \times 10^{-4} \text{ cm}^2$.

Fig. B11. As in Figure 10, for a FATFET fabricated on the same wafer as the device of Figure 9.

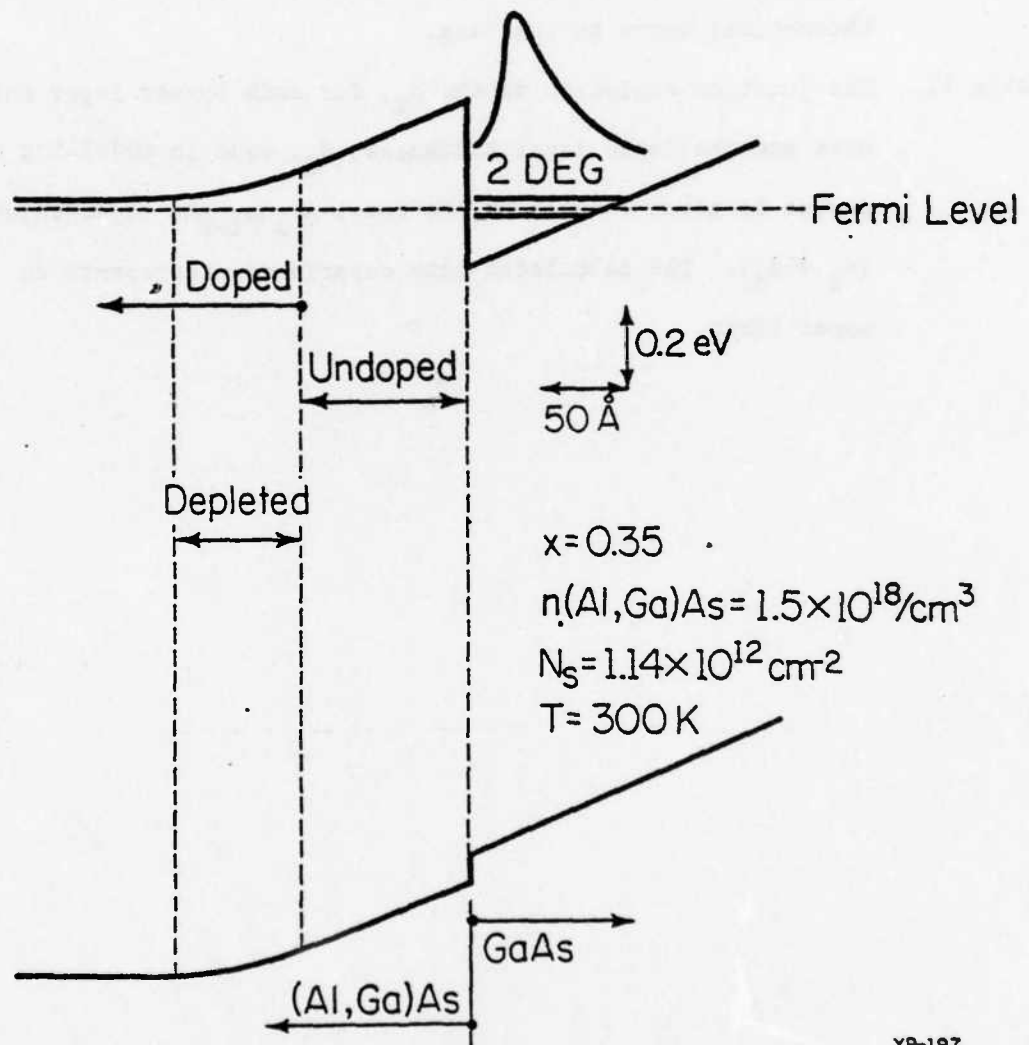
Fig. B12. Drain I-V characteristic of a device with a back-to-back diode gate. The p^+ doping is about $1.6 \times 10^{19} \text{ cm}^{-3}$.

Fig. B13. Maximum available gain vs. frequency for a CAMFET similar to that of Figure 8.

TABLE CAPTIONS

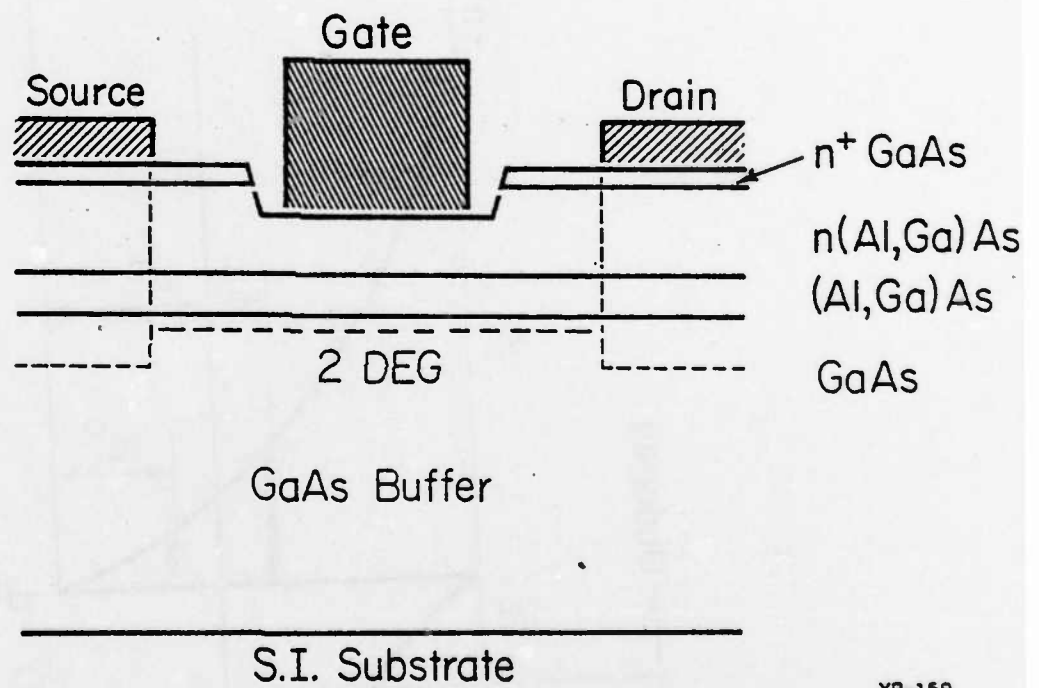
Table I. Measured and theoretical maximum values of transconductance and saturation current. Theoretical values are in parentheses. The values of source resistances are those employed in fitting the theoretical curve to the data.

Table II. The junction depletion depth, d_i , for each spacer layer thickness and the doped layer thickness, d_d , used in modelling each device is given as well as the total $\text{Al}_x\text{Ga}_{1-x}\text{As}$ layer thickness ($d_i + d_d$). The calculated gate capacitance represents an upper limit.



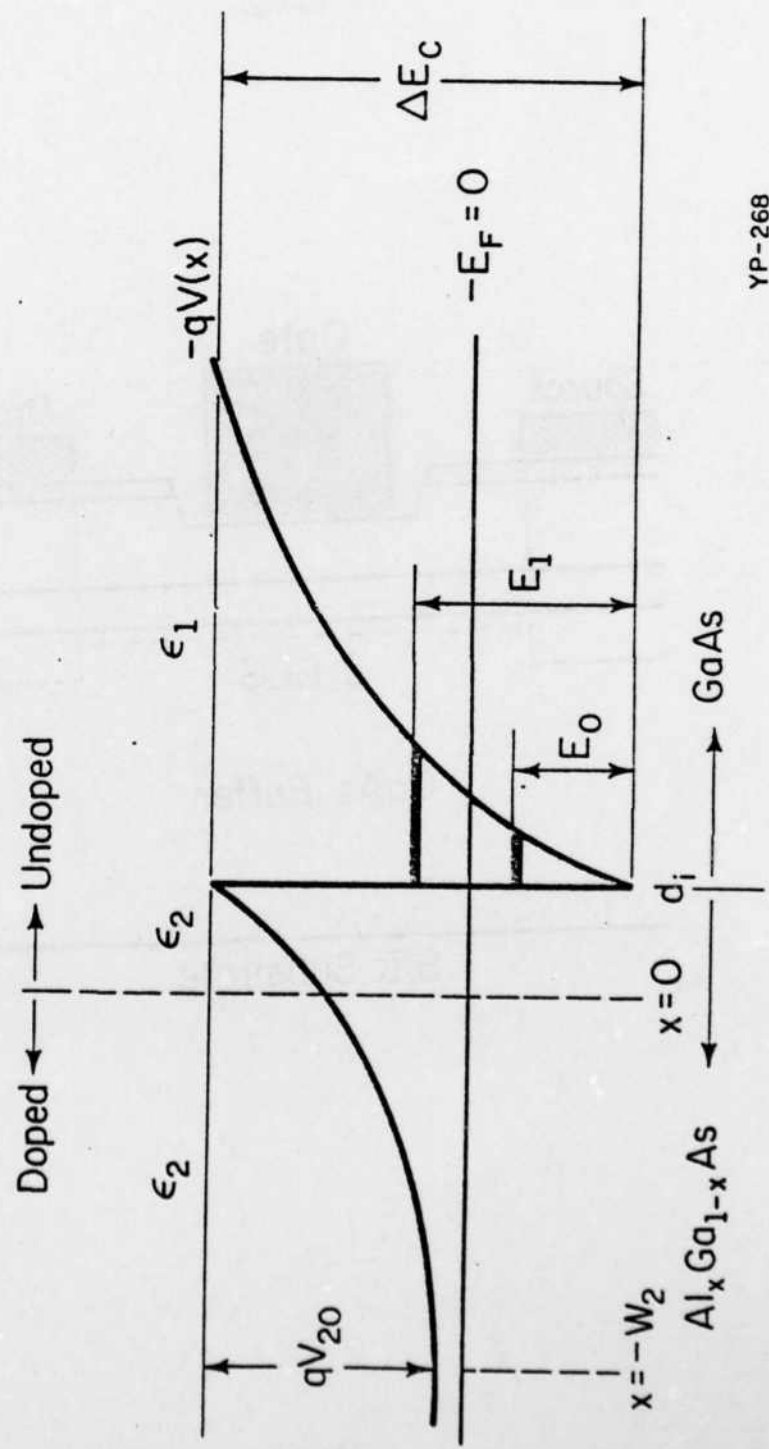
YP-197

Fig. 1



YP-159

Fig. 2



YP-268

Fig. 3

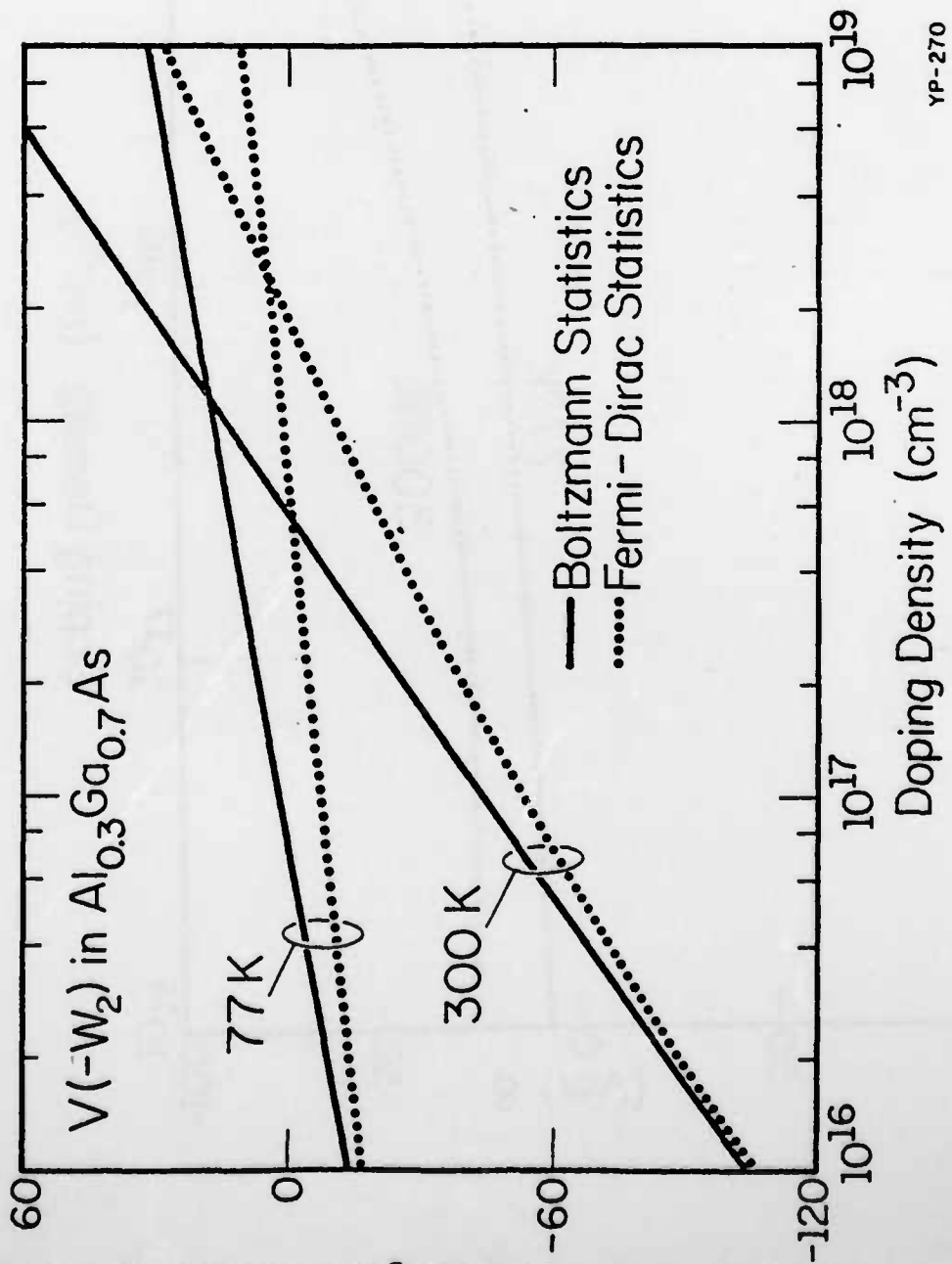
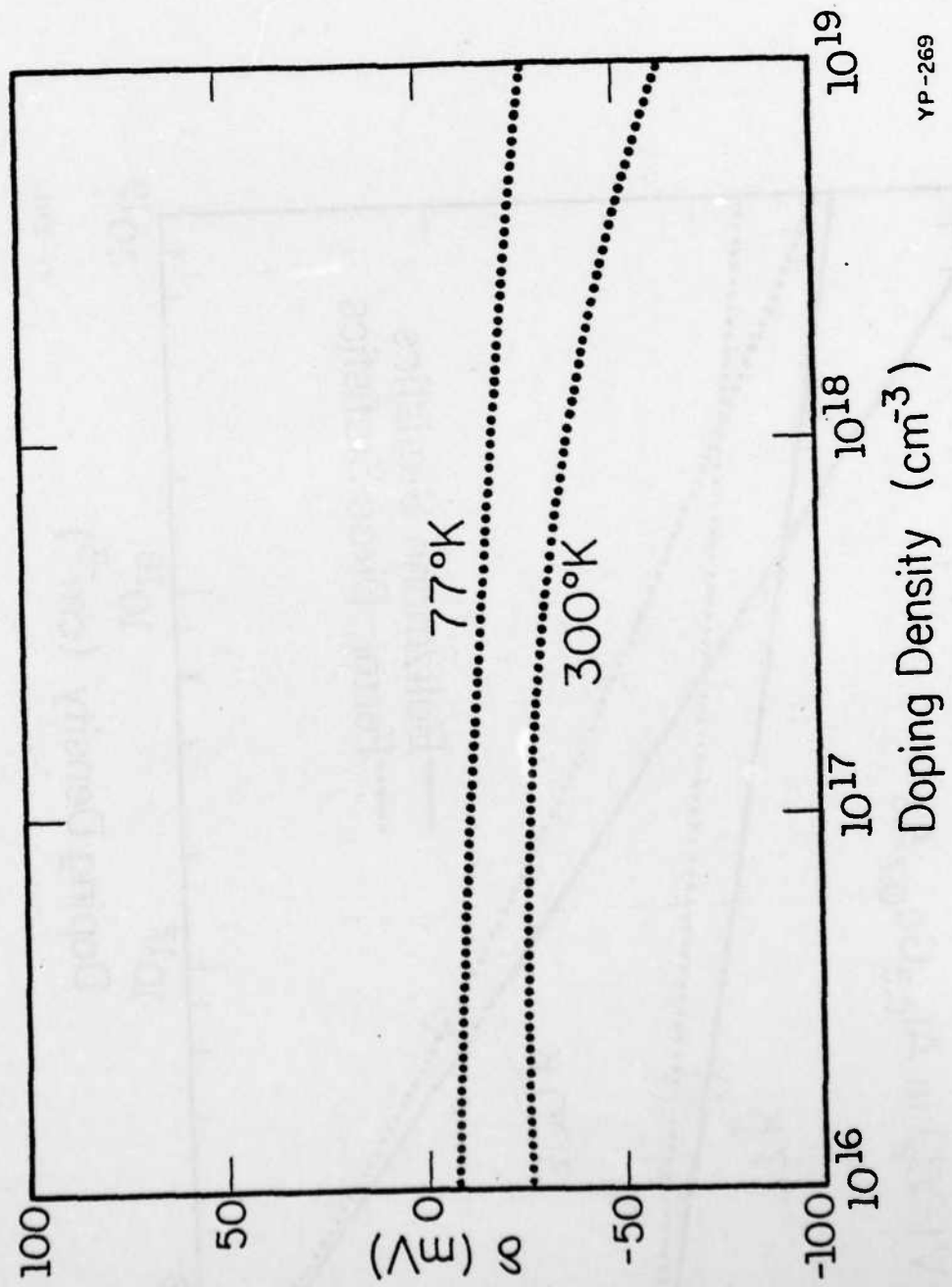


Fig. 4



YP-269

Fig. 5

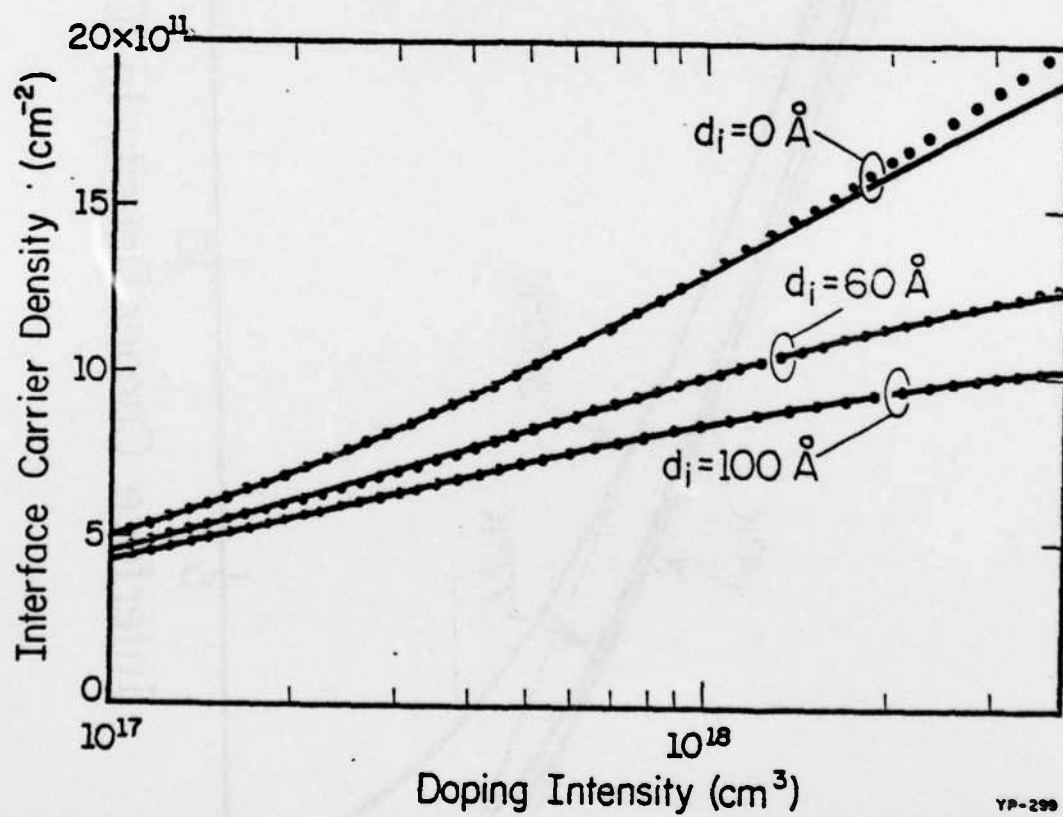


Fig. 6

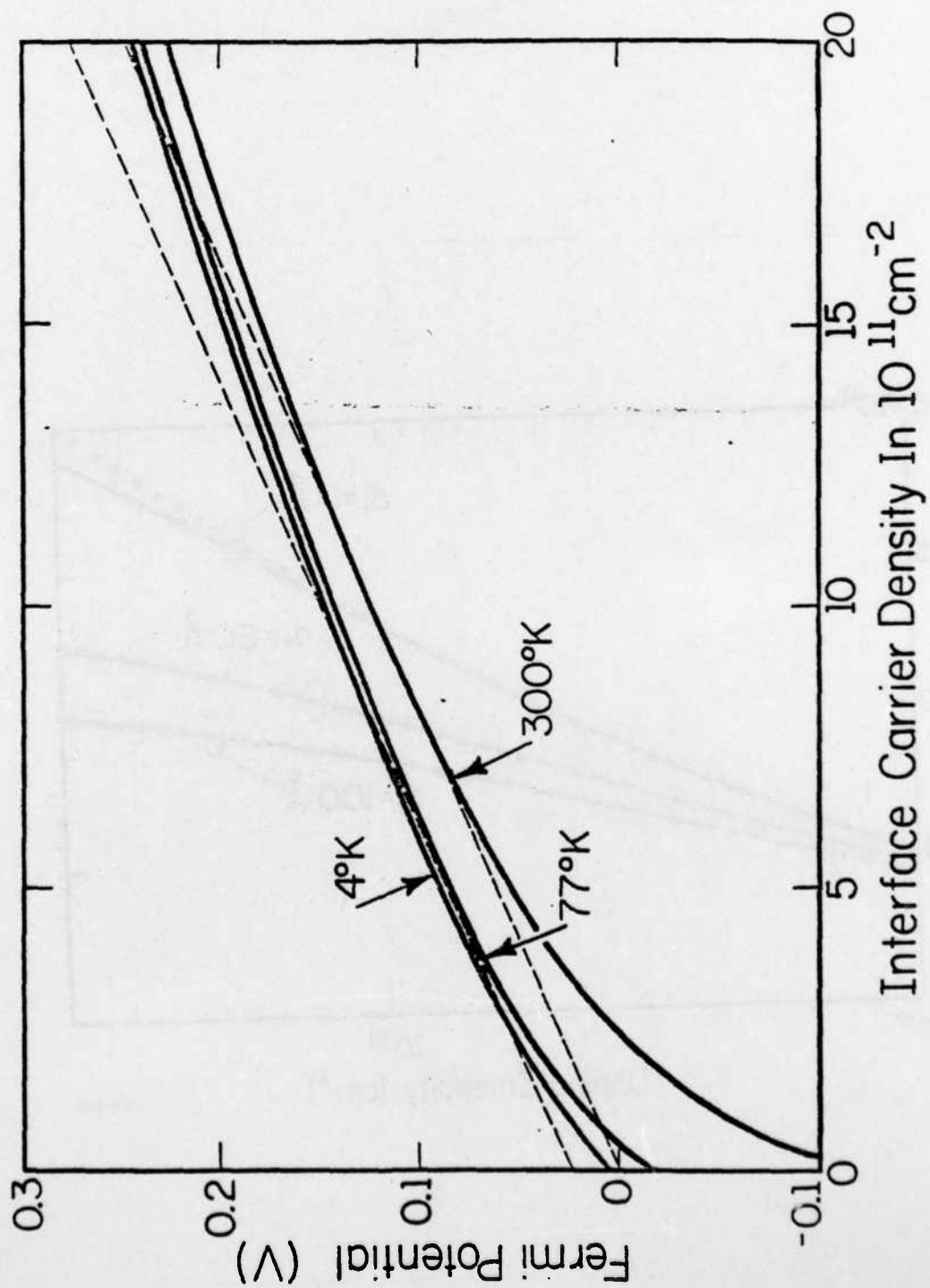


Fig. 7

YP-232

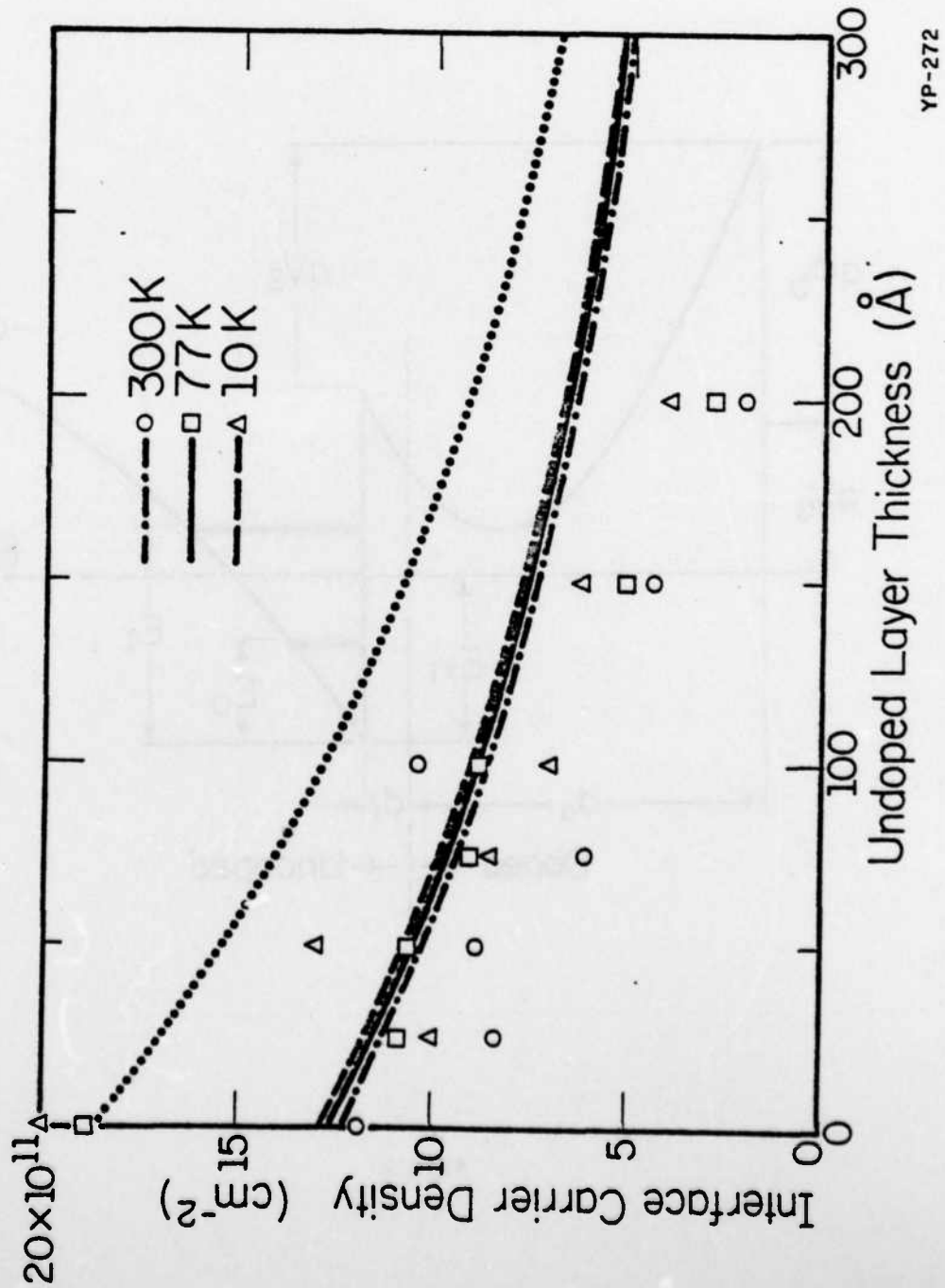
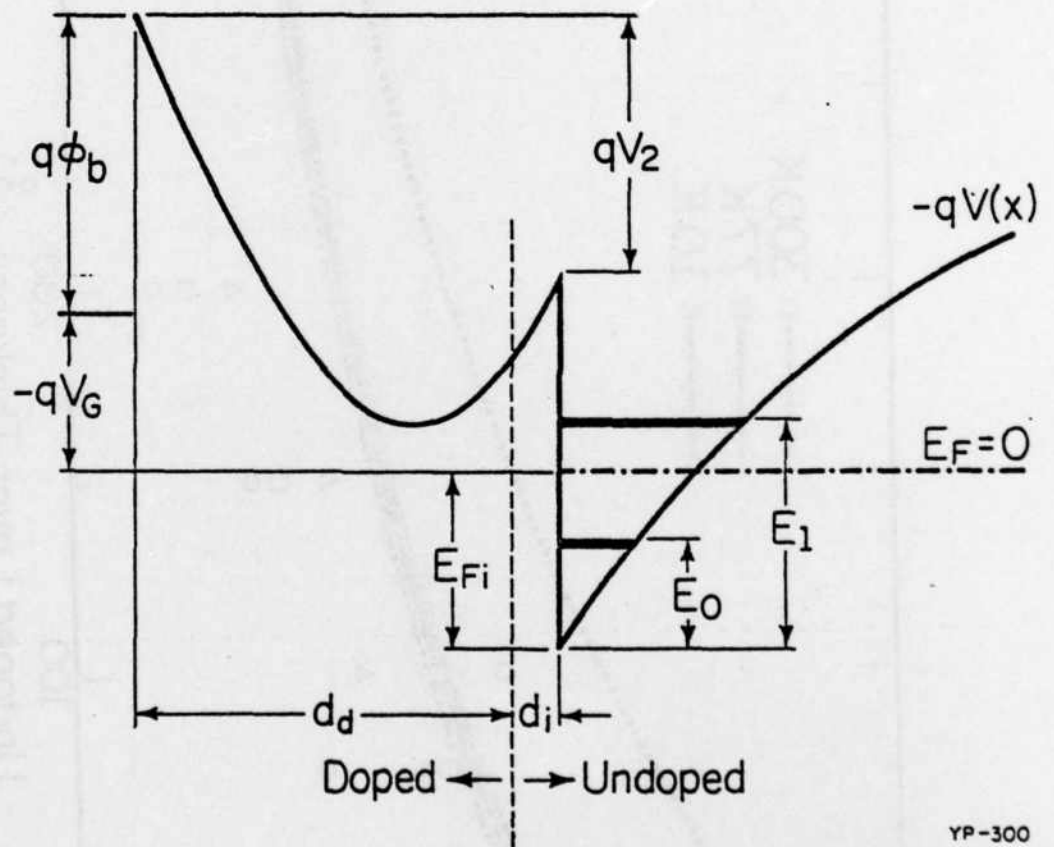
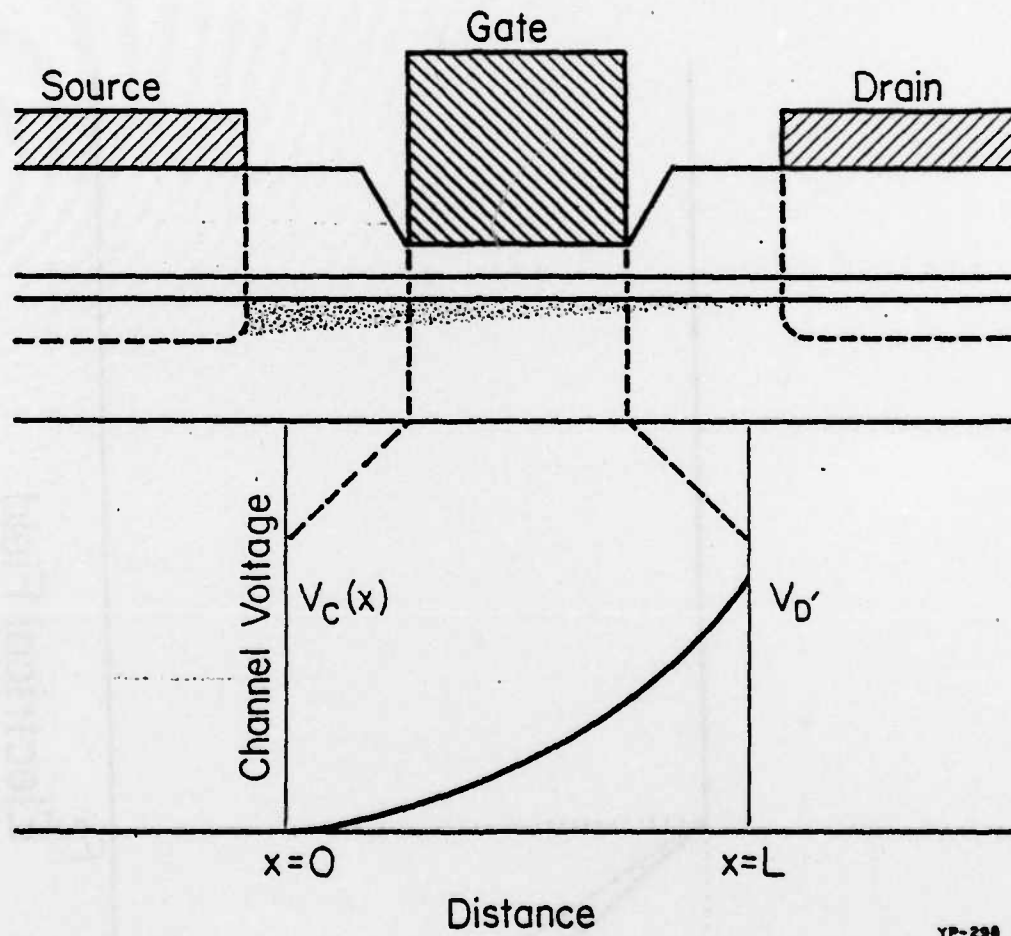


Fig. 8



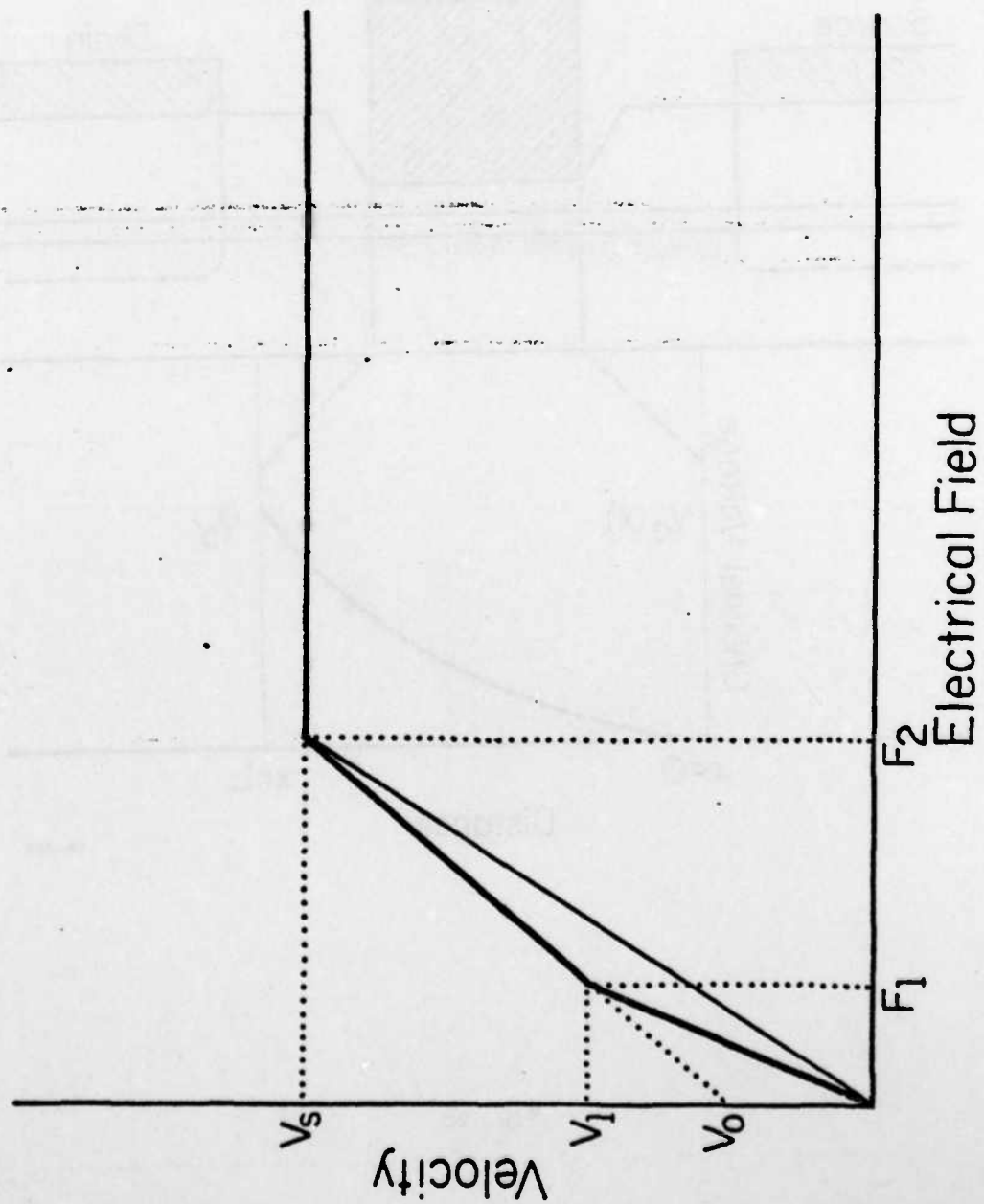
YP-300

Fig. 9

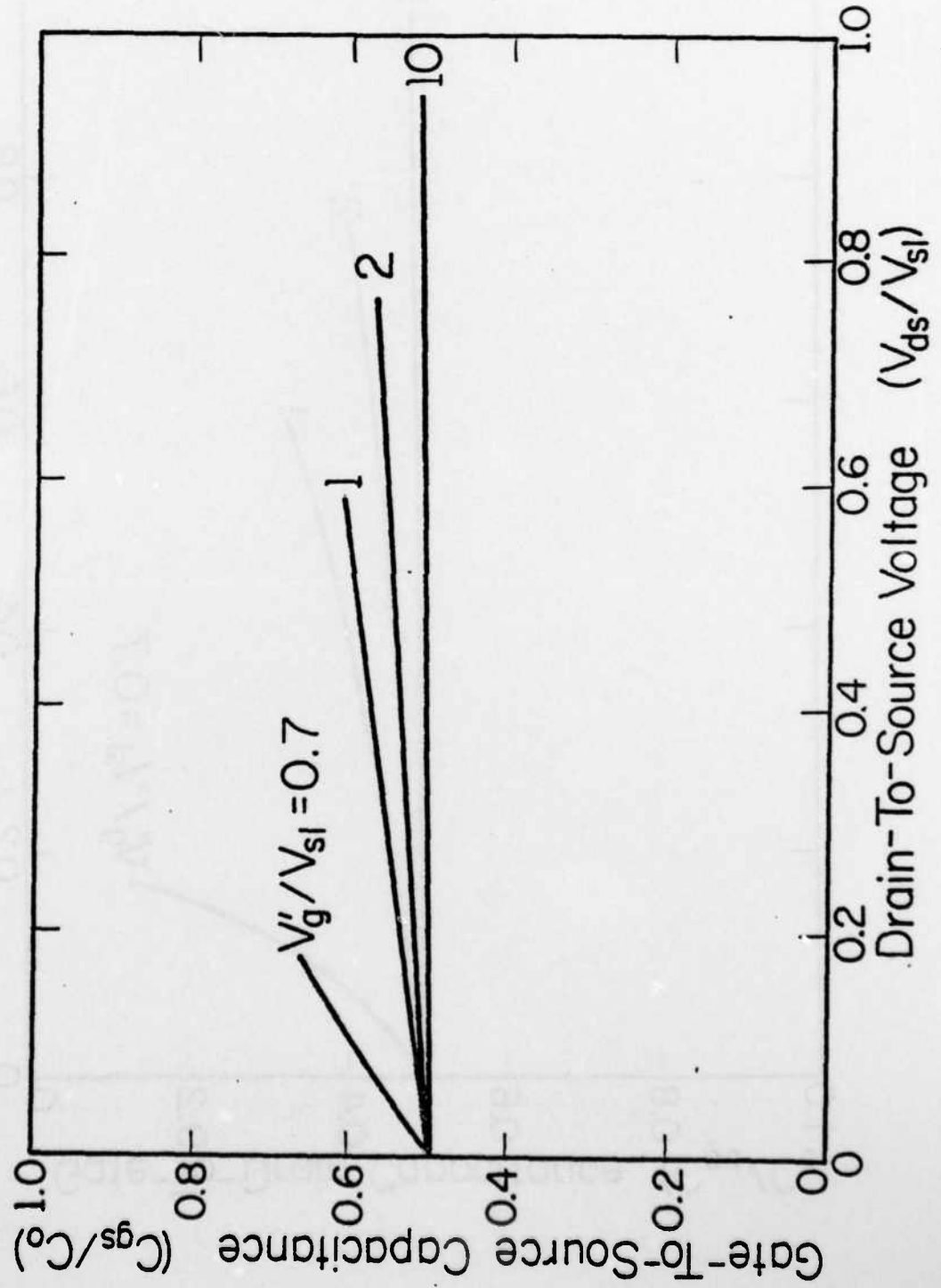


YP-298

Fig. 10

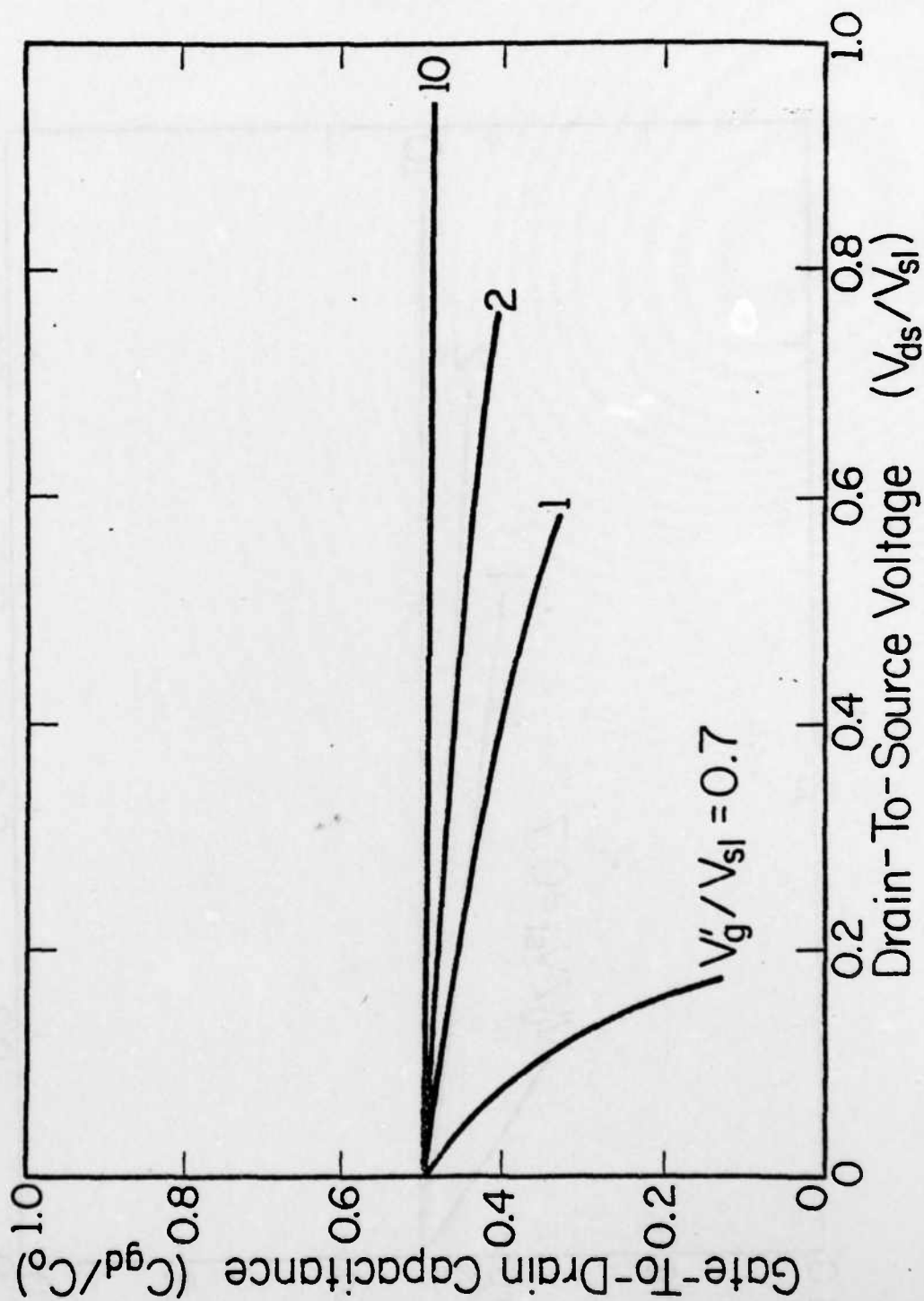


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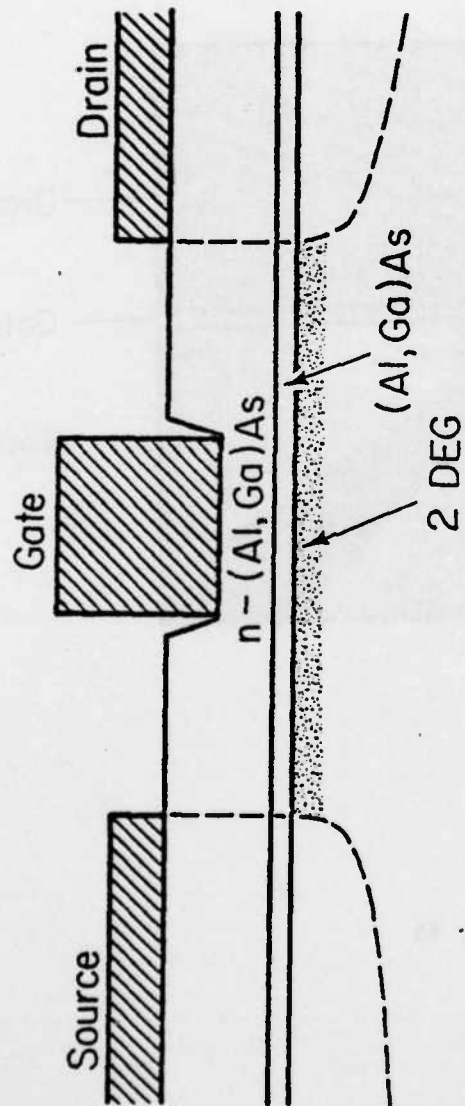
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Fig. 12



YP-236

Fig. 13



S. I. Substrate

YP-266

Fig. 14

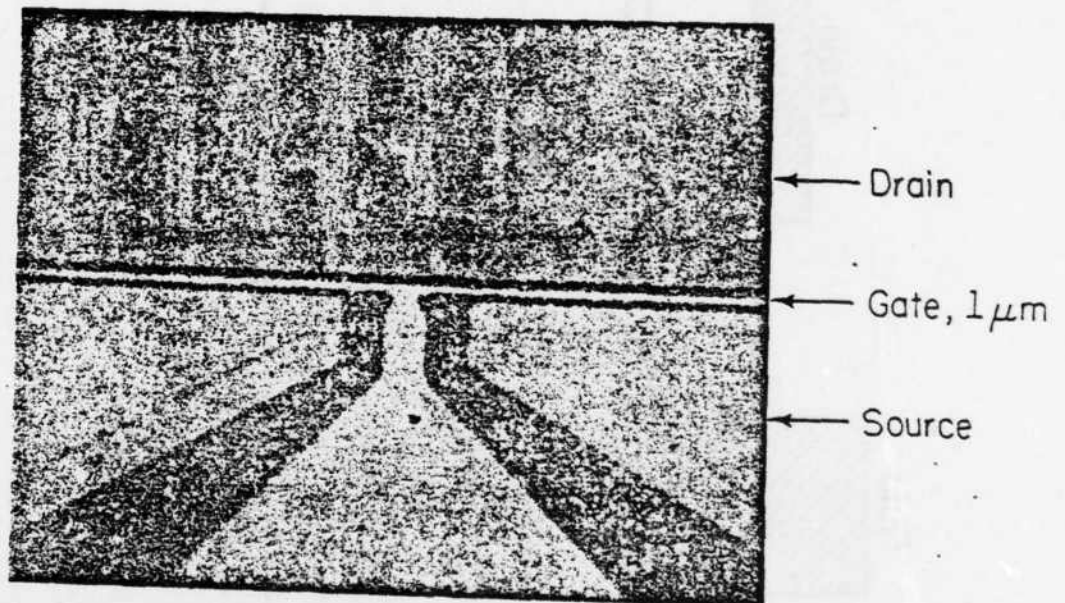


Fig. 15

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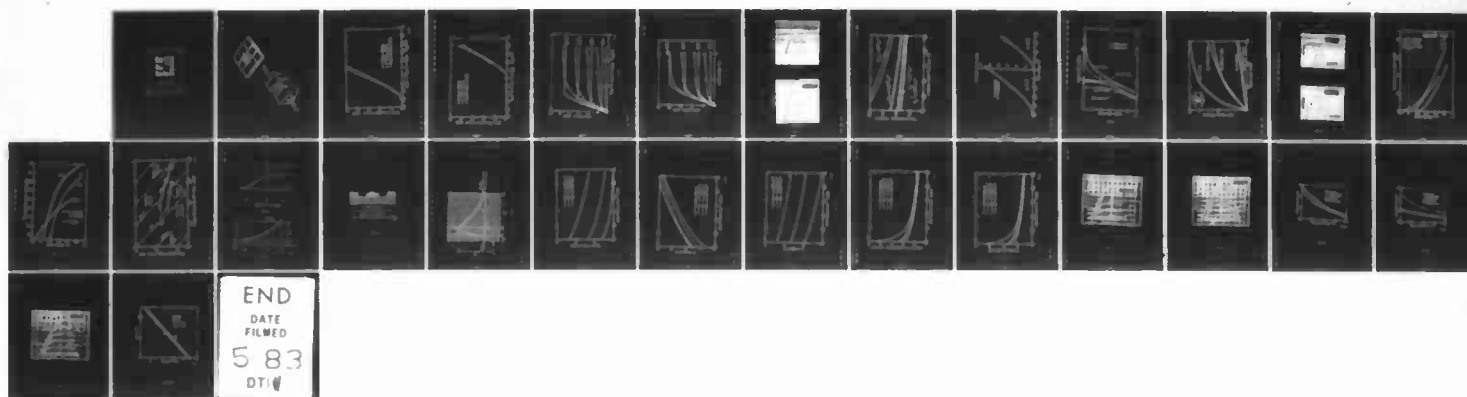
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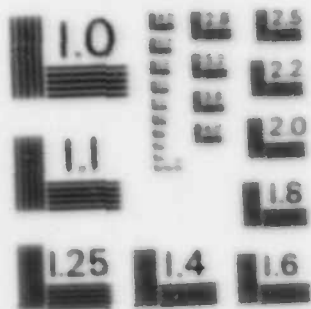
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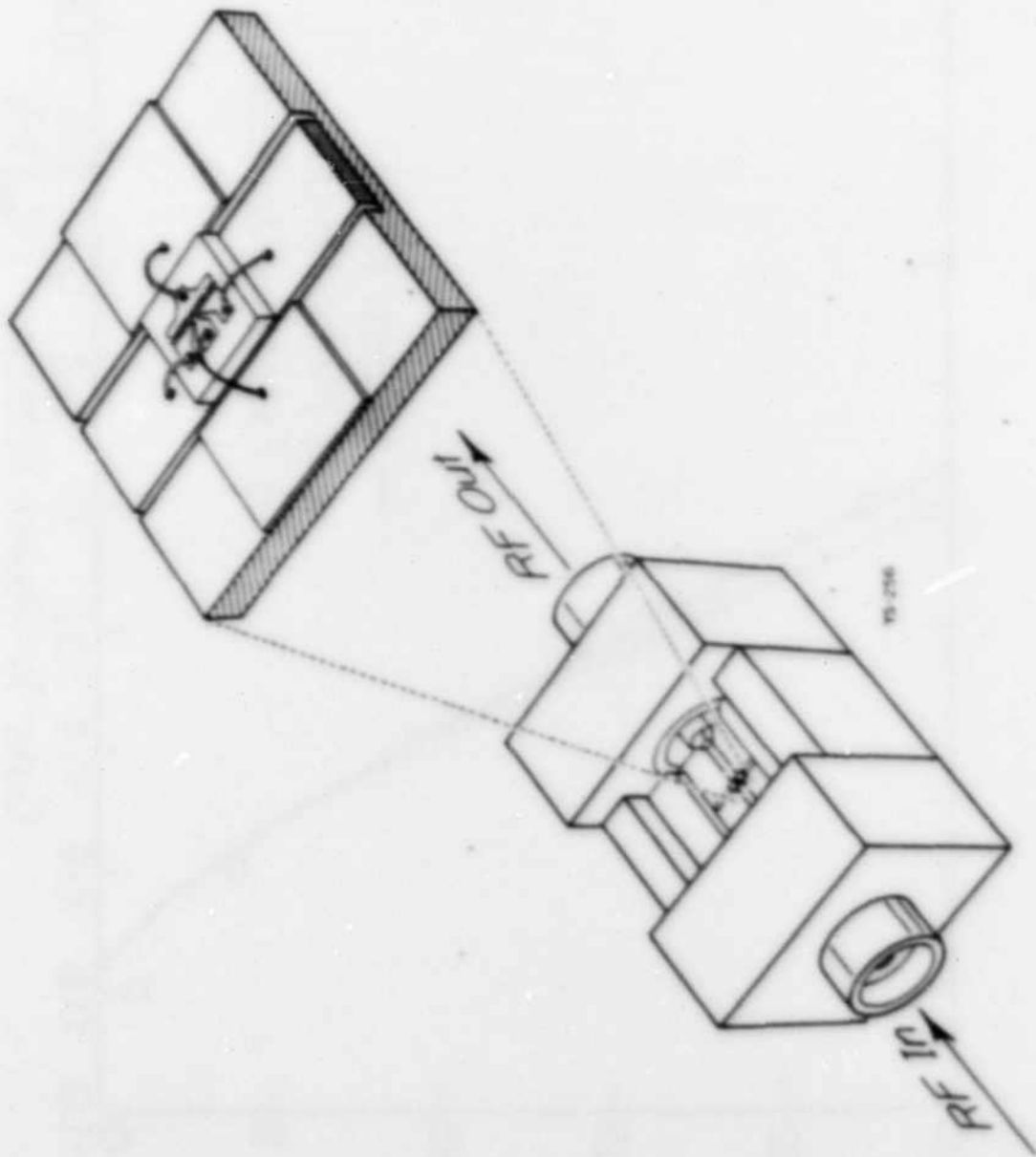
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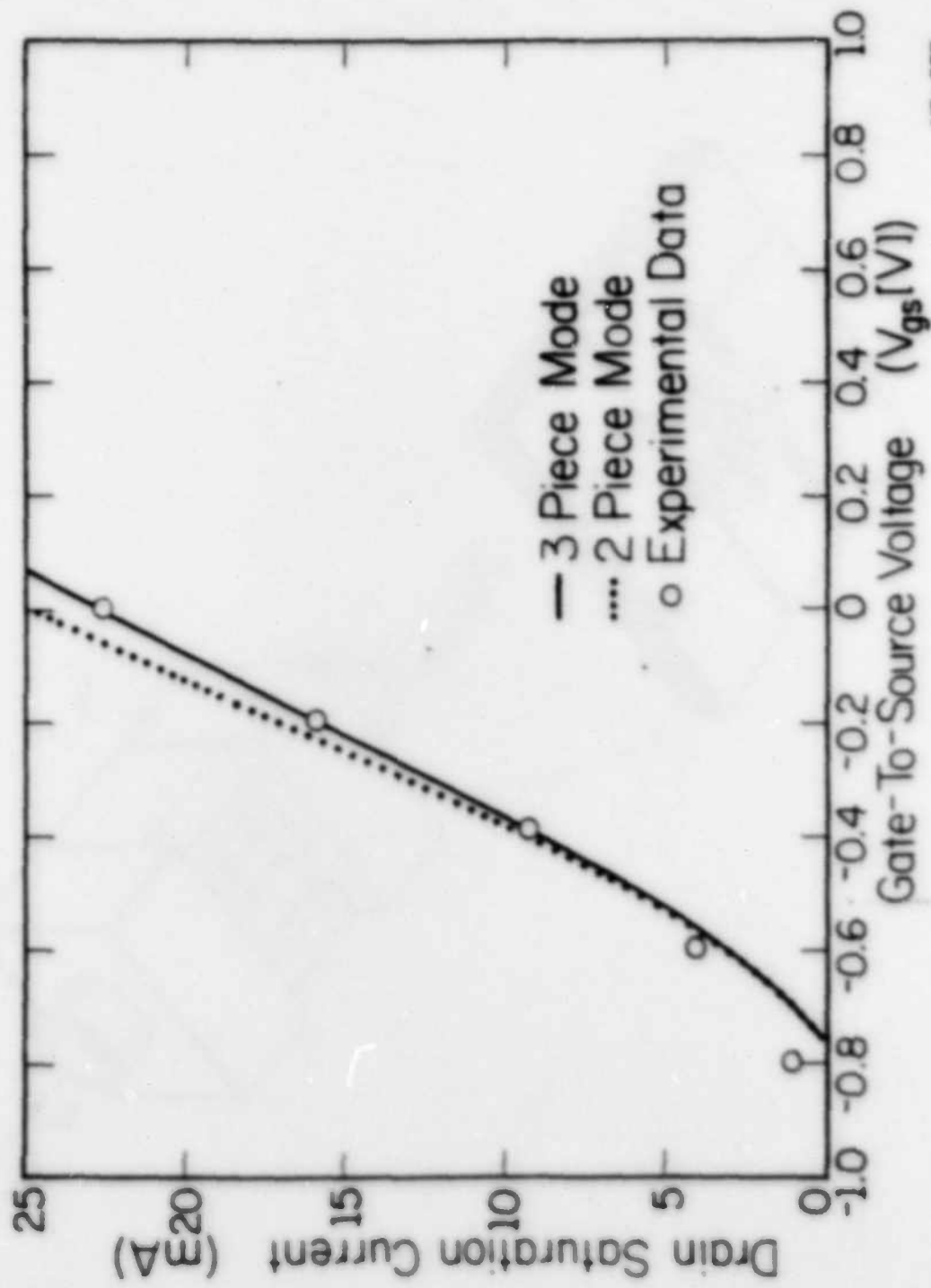
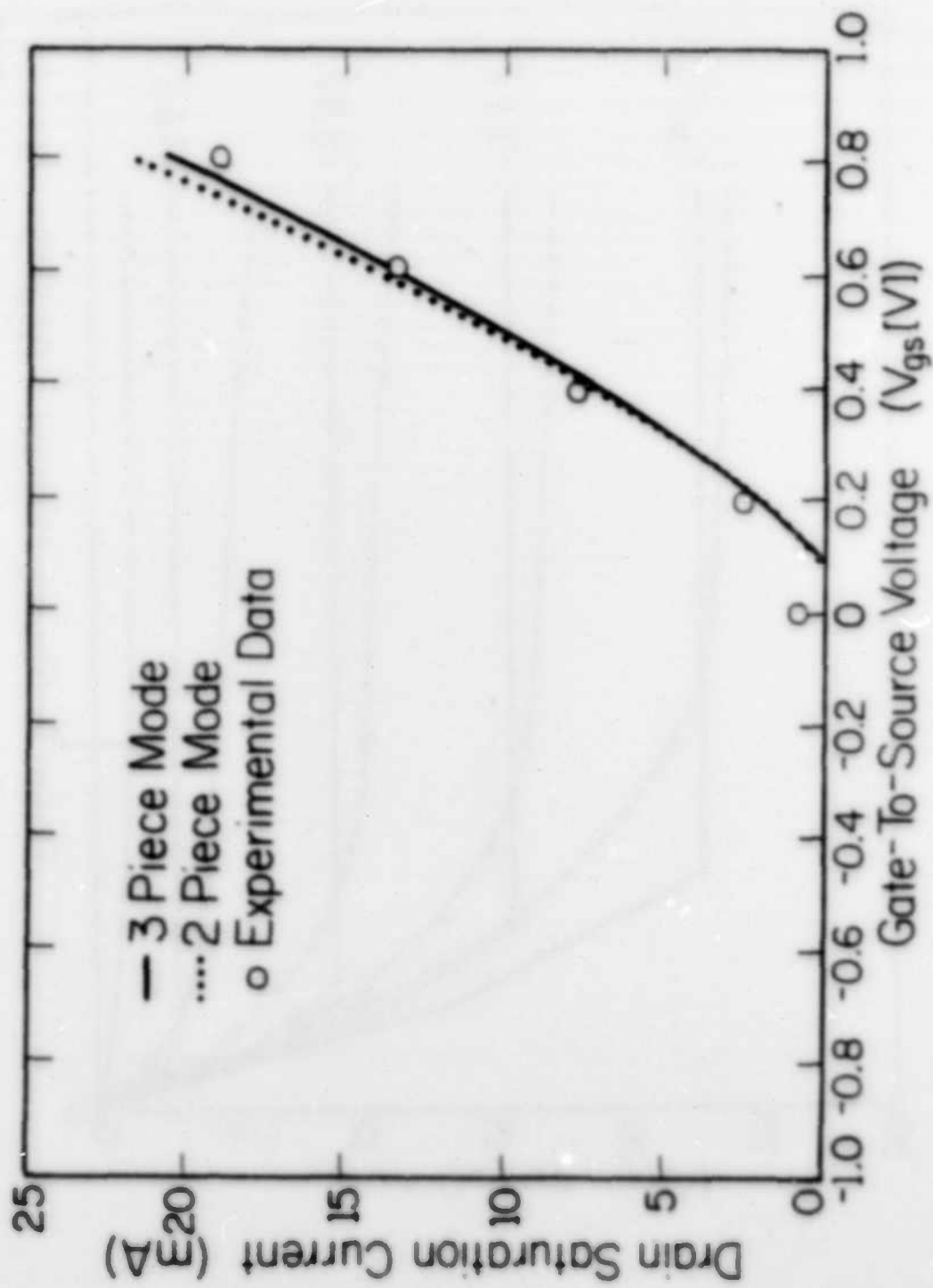
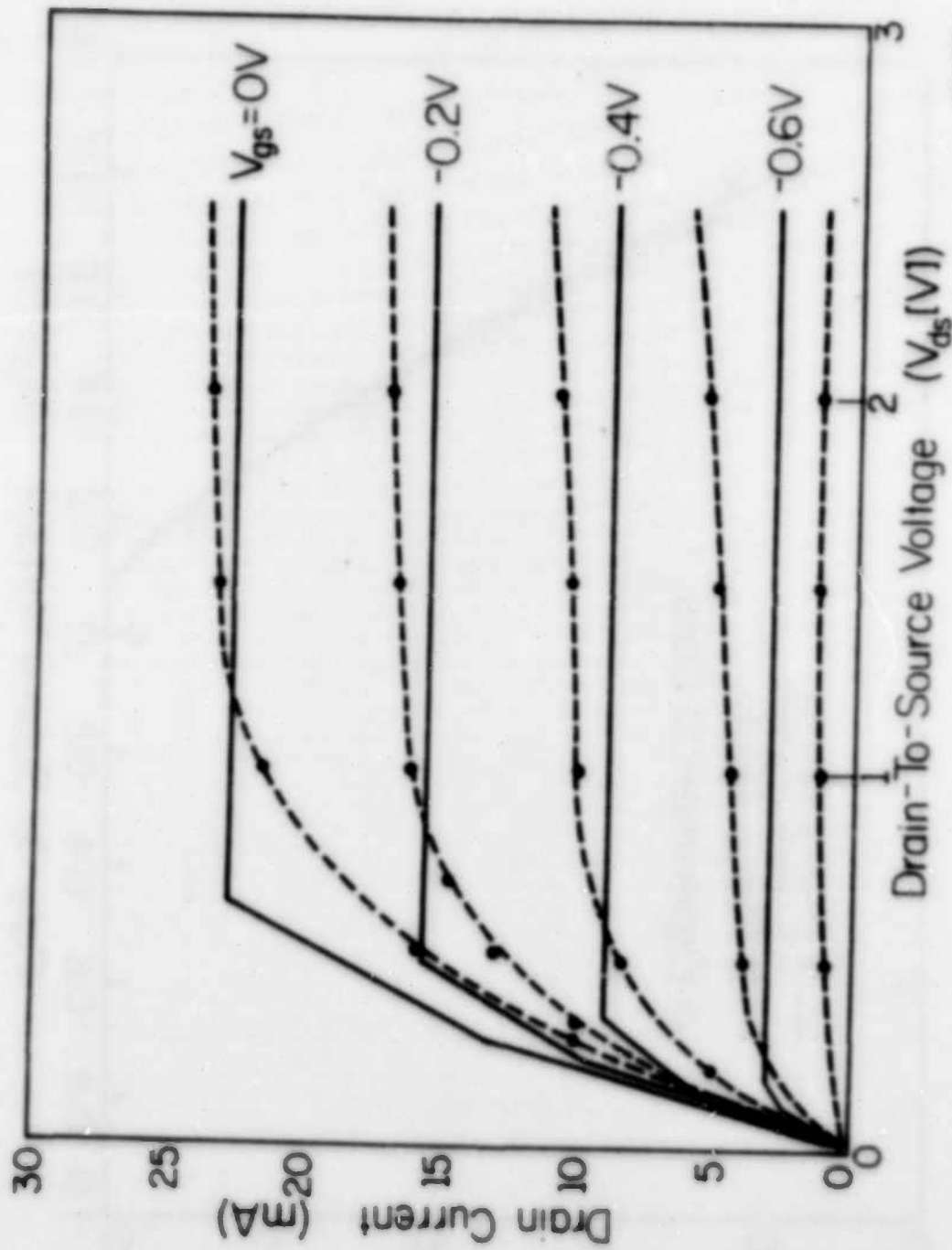


Fig. 17



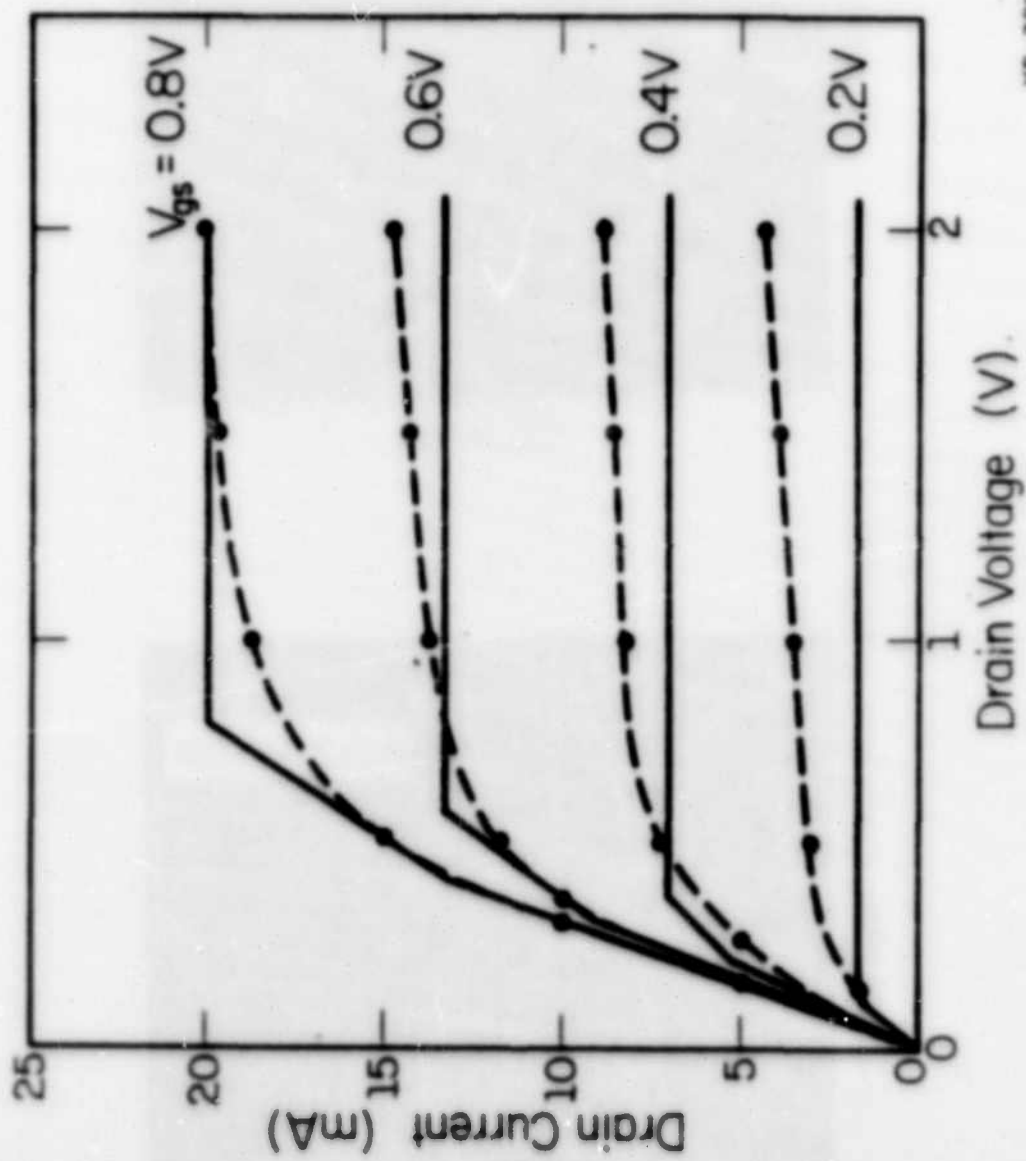
YP-238

Fig. 18



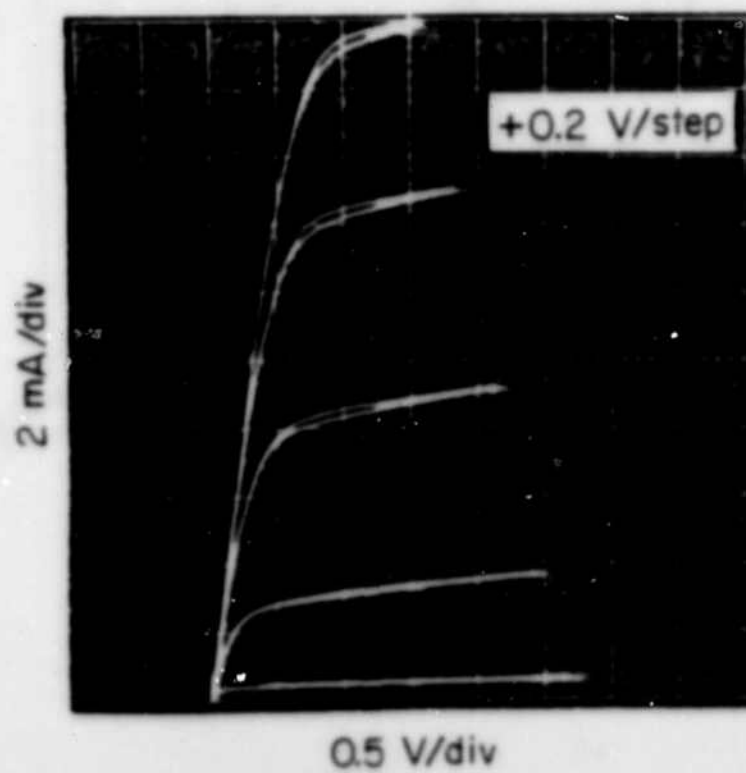
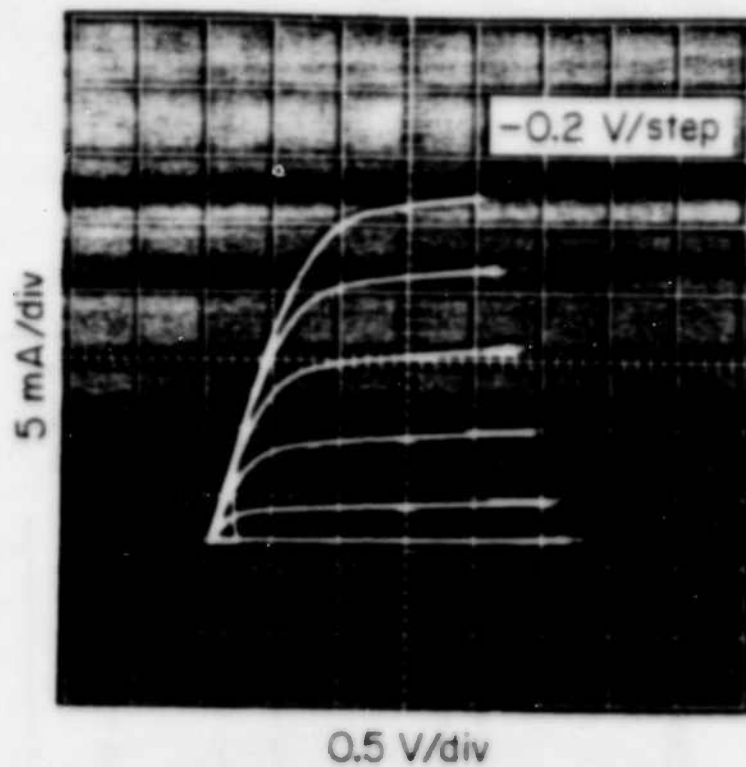
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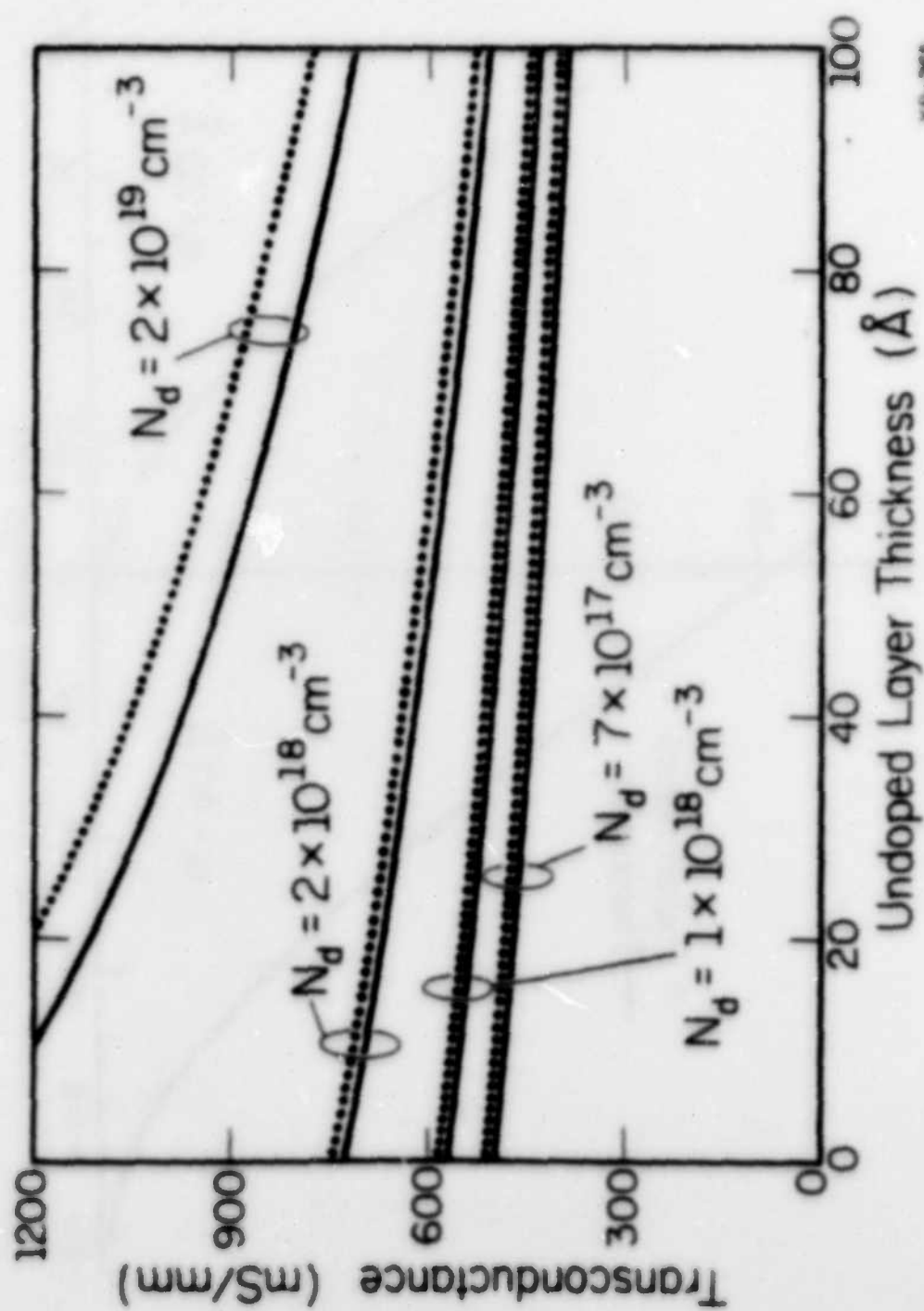
Fig. 19a



YP-306

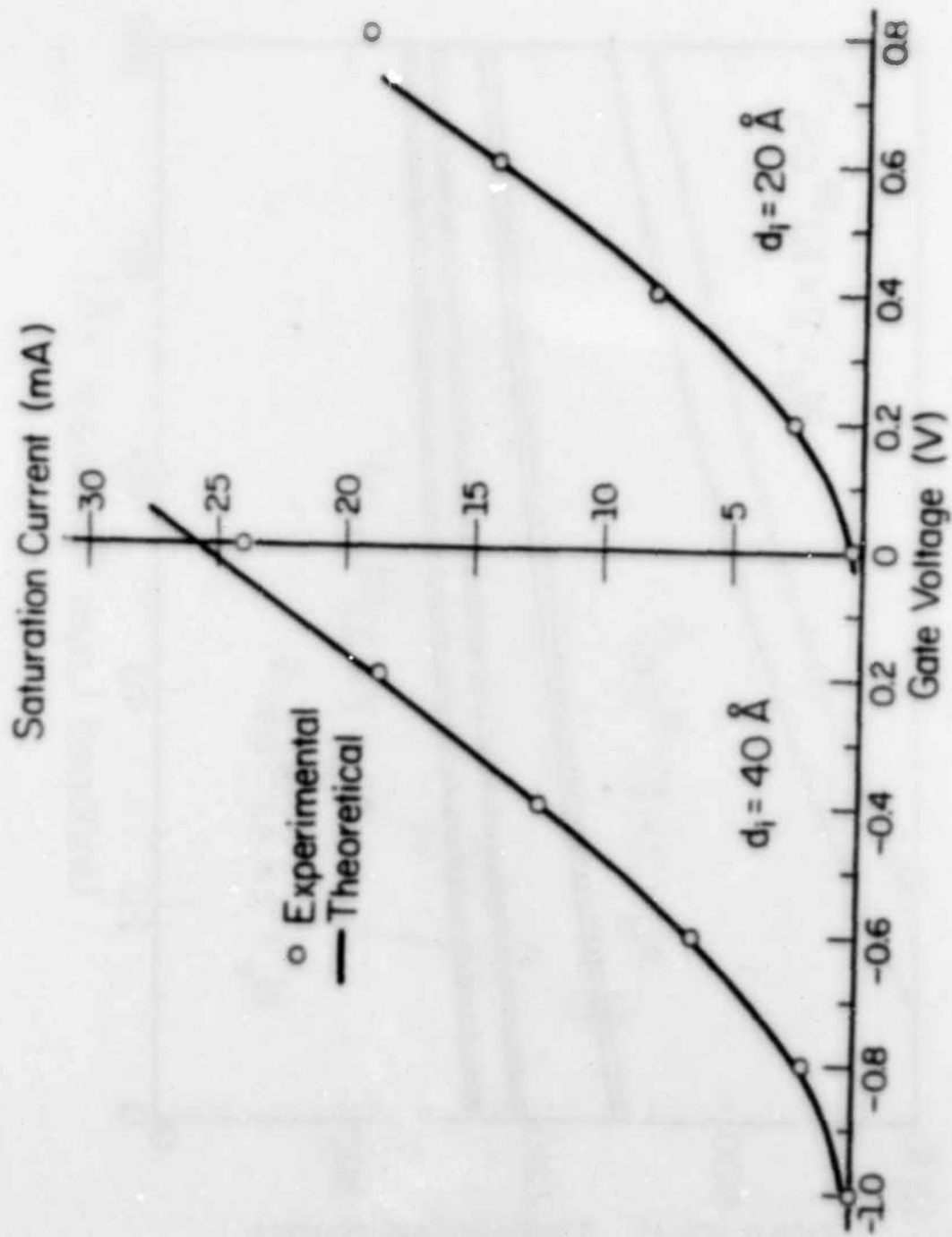
Fig. 19b





VP-265

Fig. 21



VP-226

Fig. 22

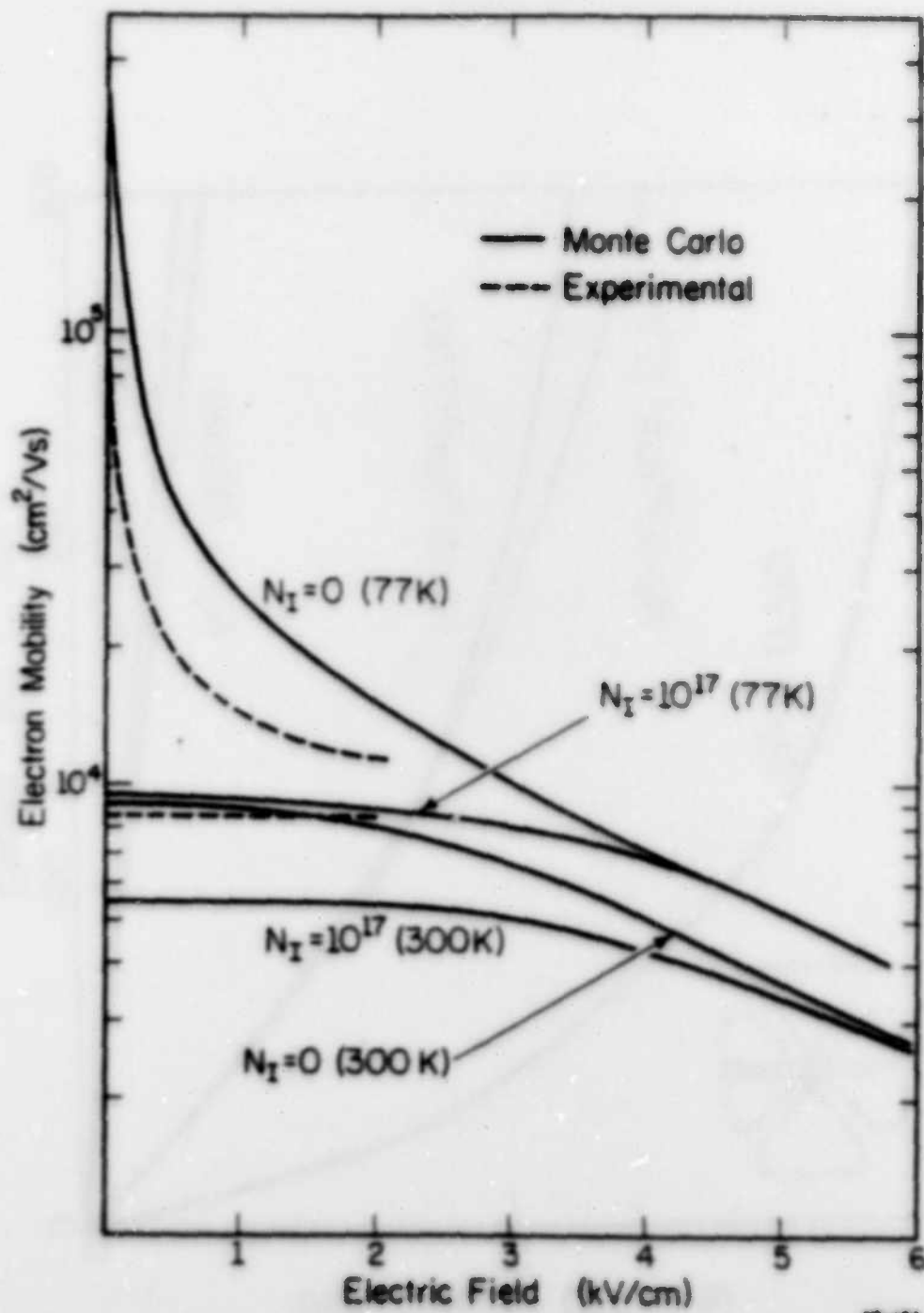


Fig. 23

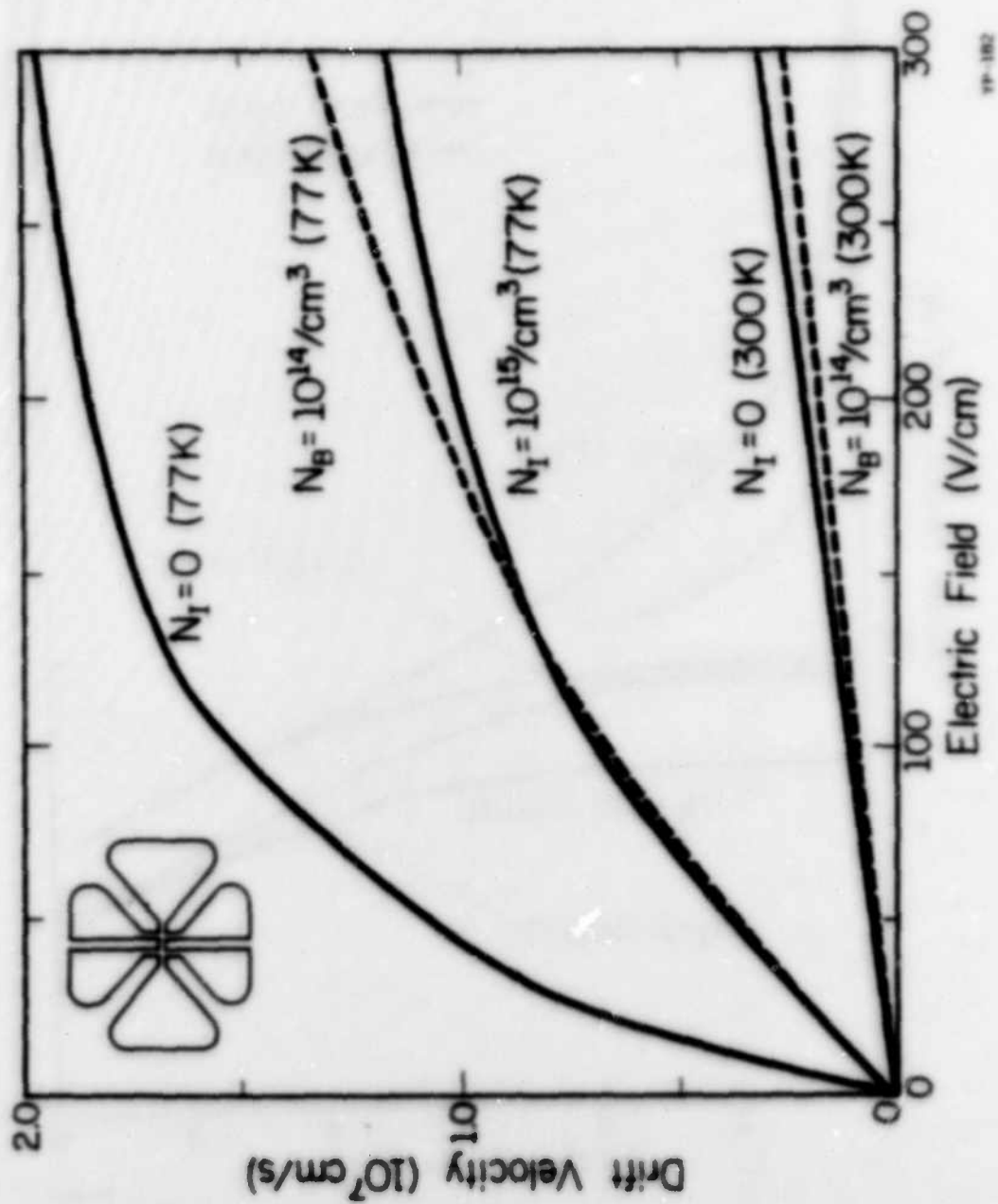


Fig. 24

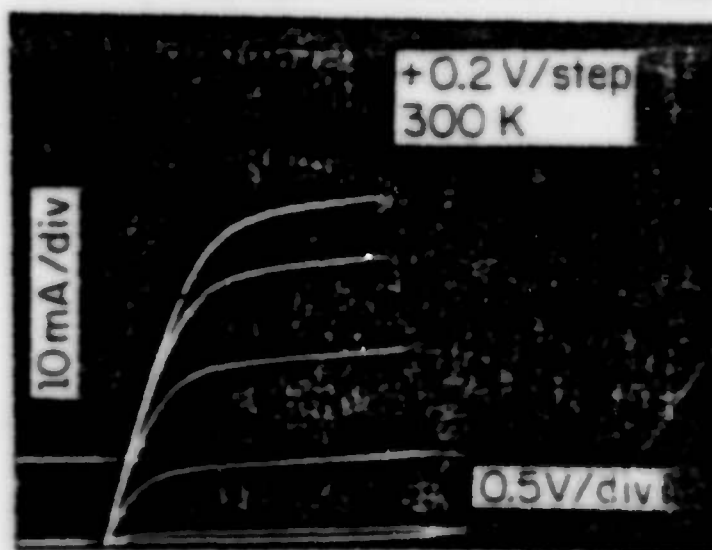
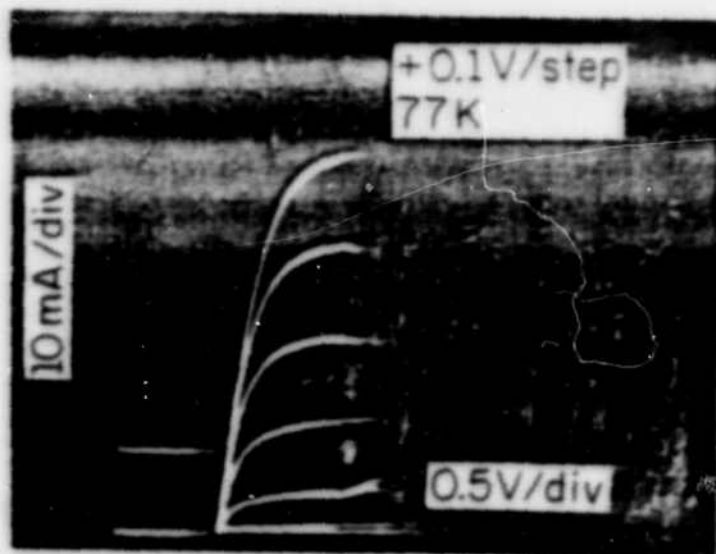


Fig. 25

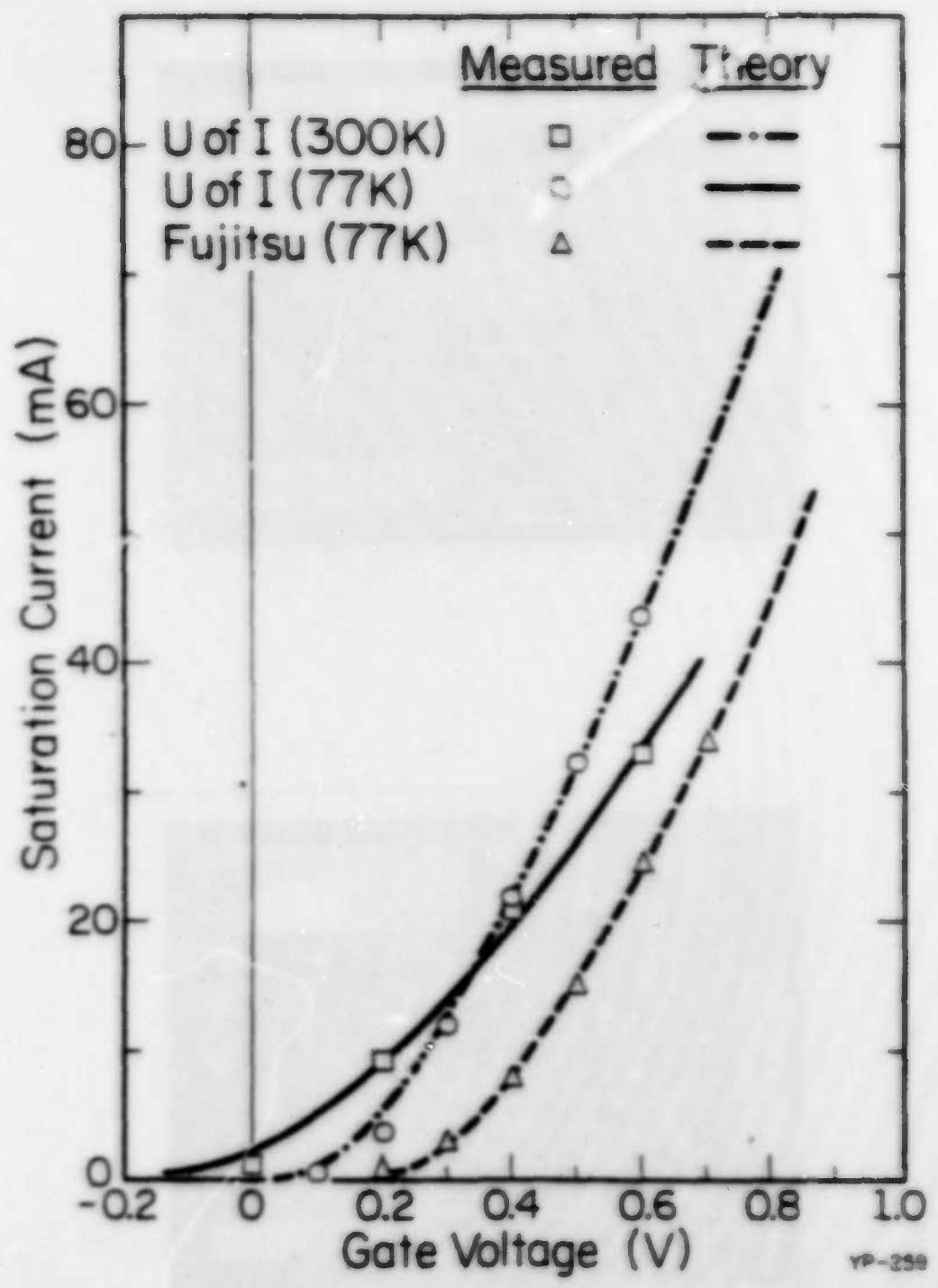


Fig. 26

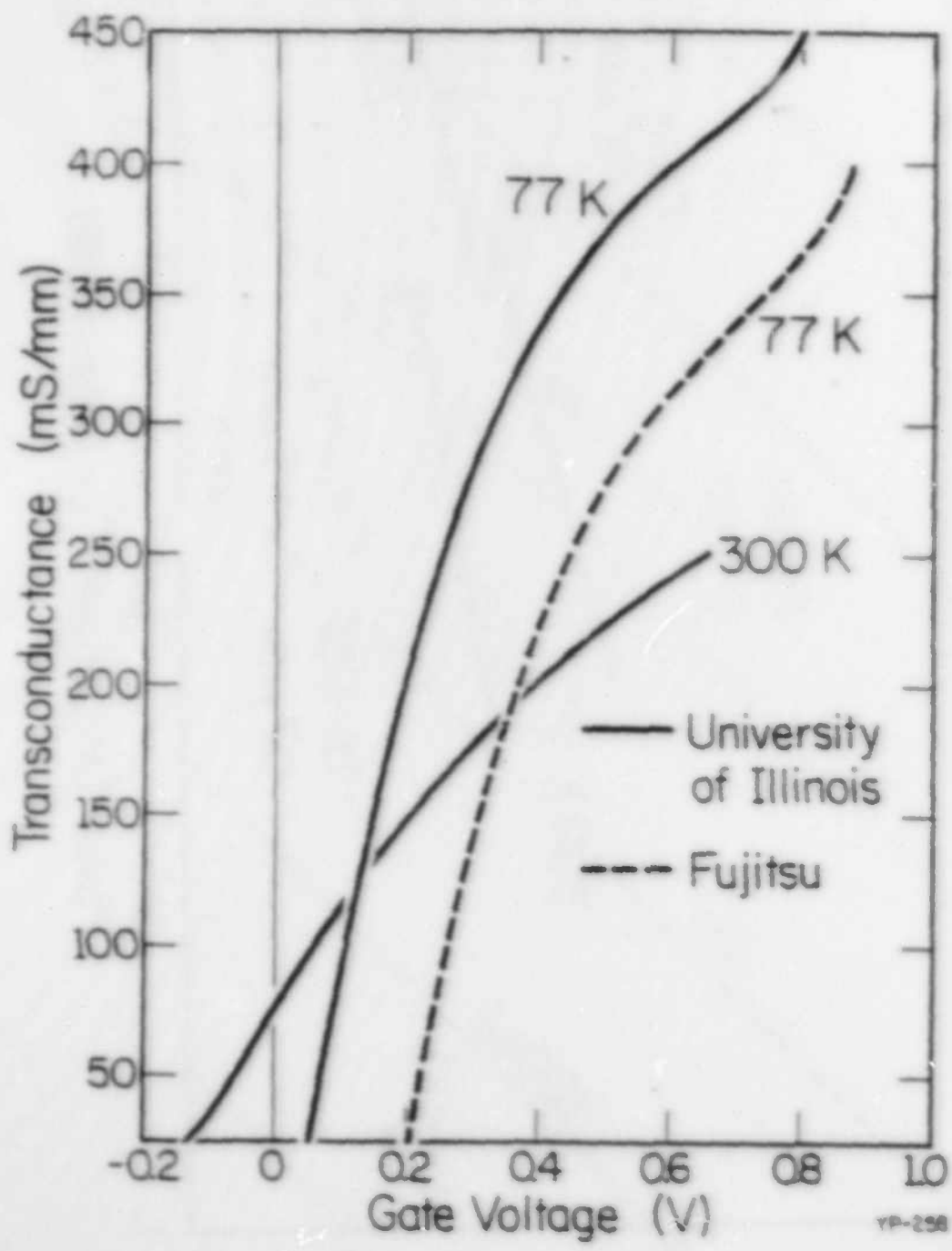


Fig. 27

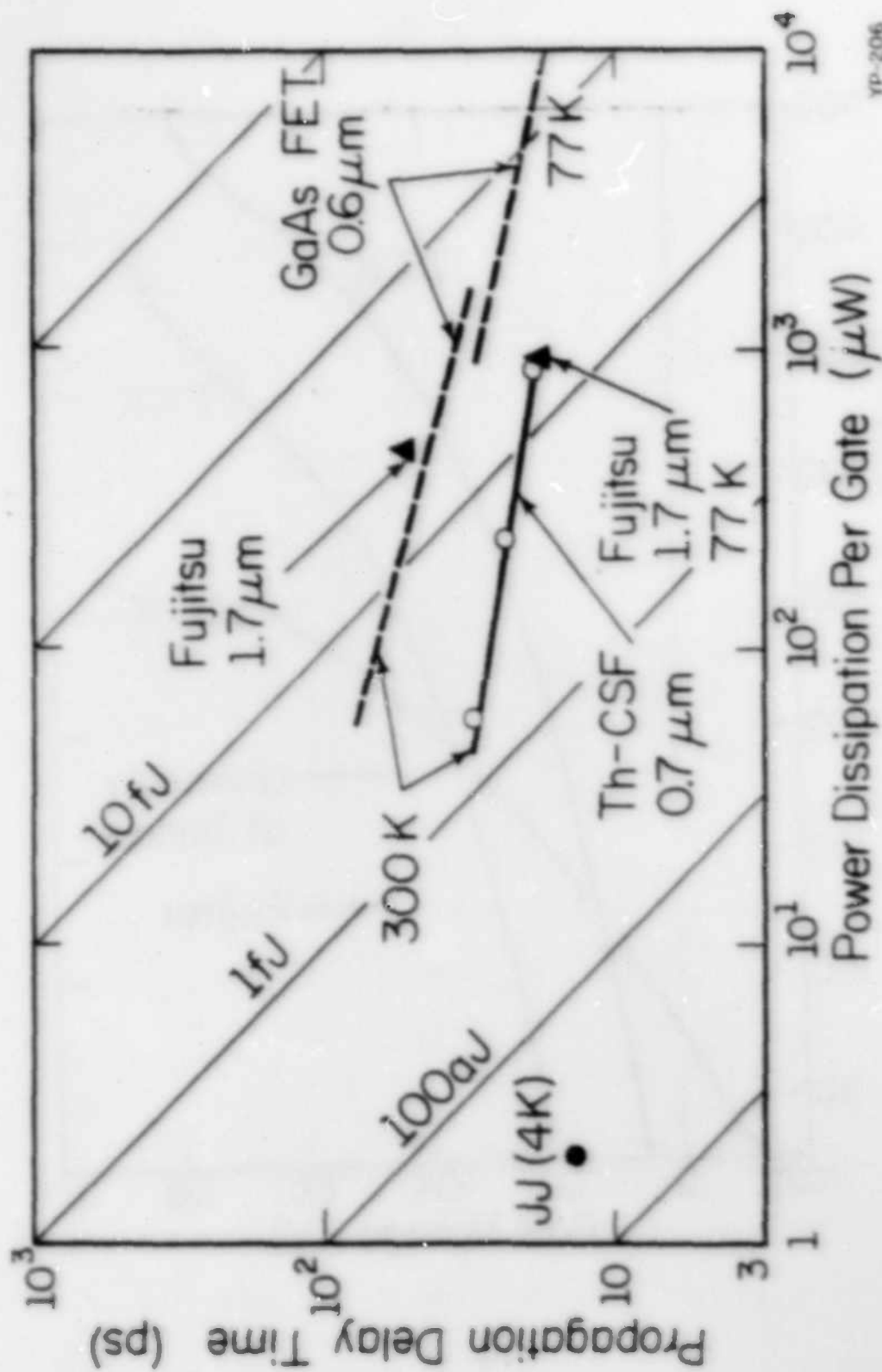


Fig. 28

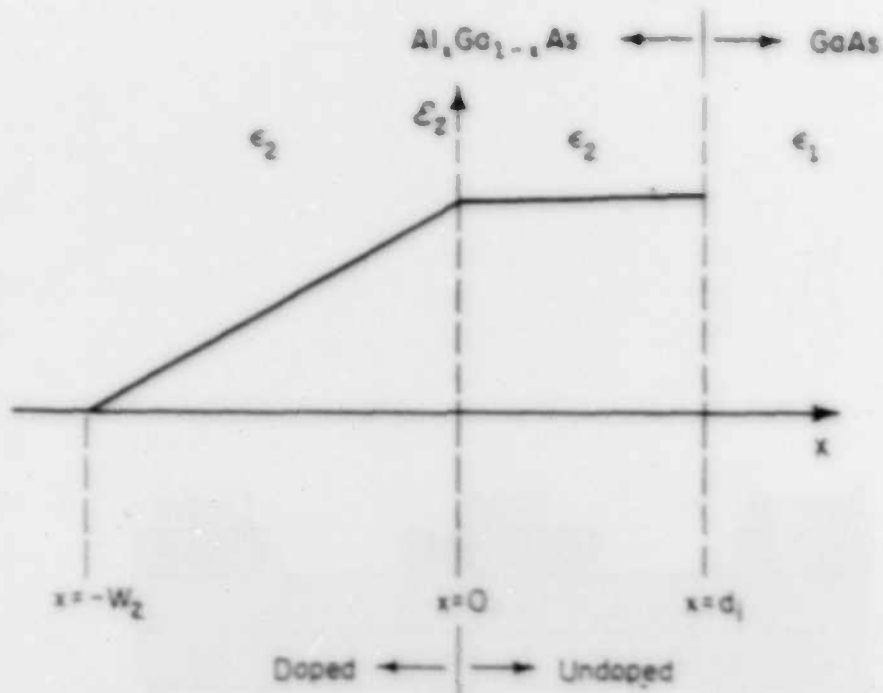


Fig. A1

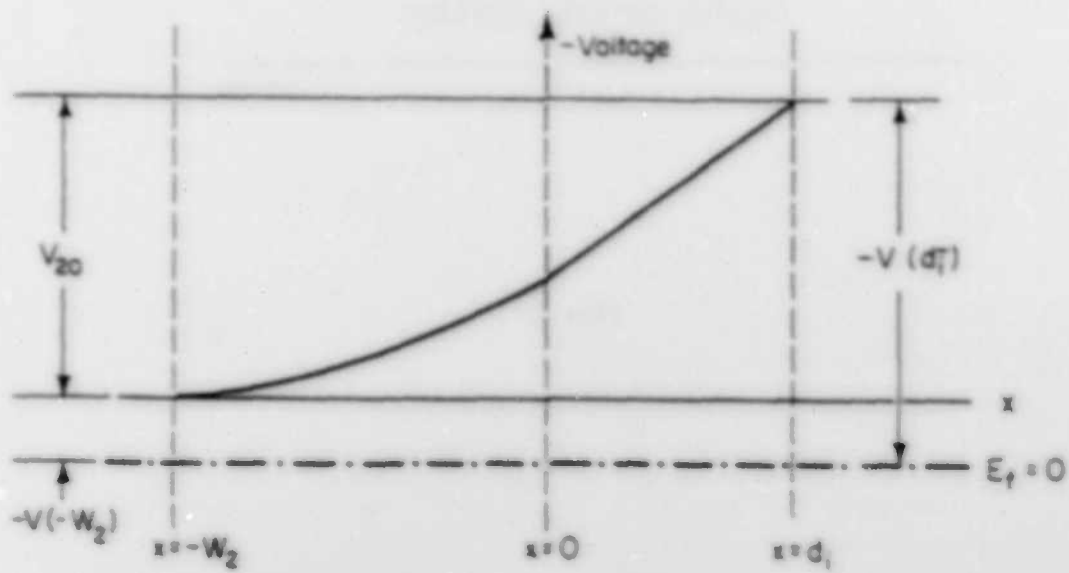
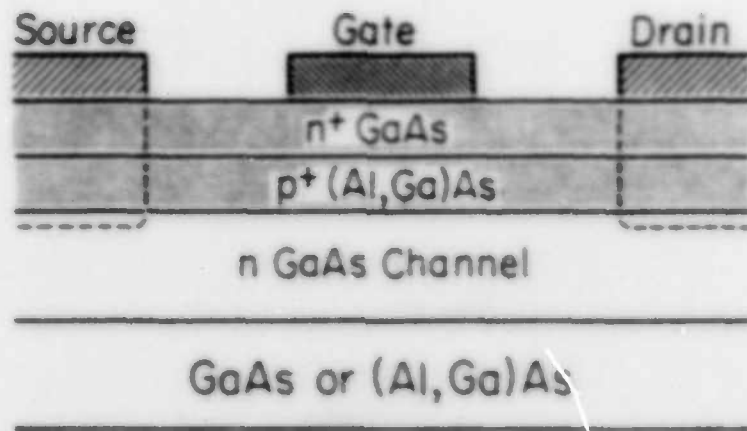
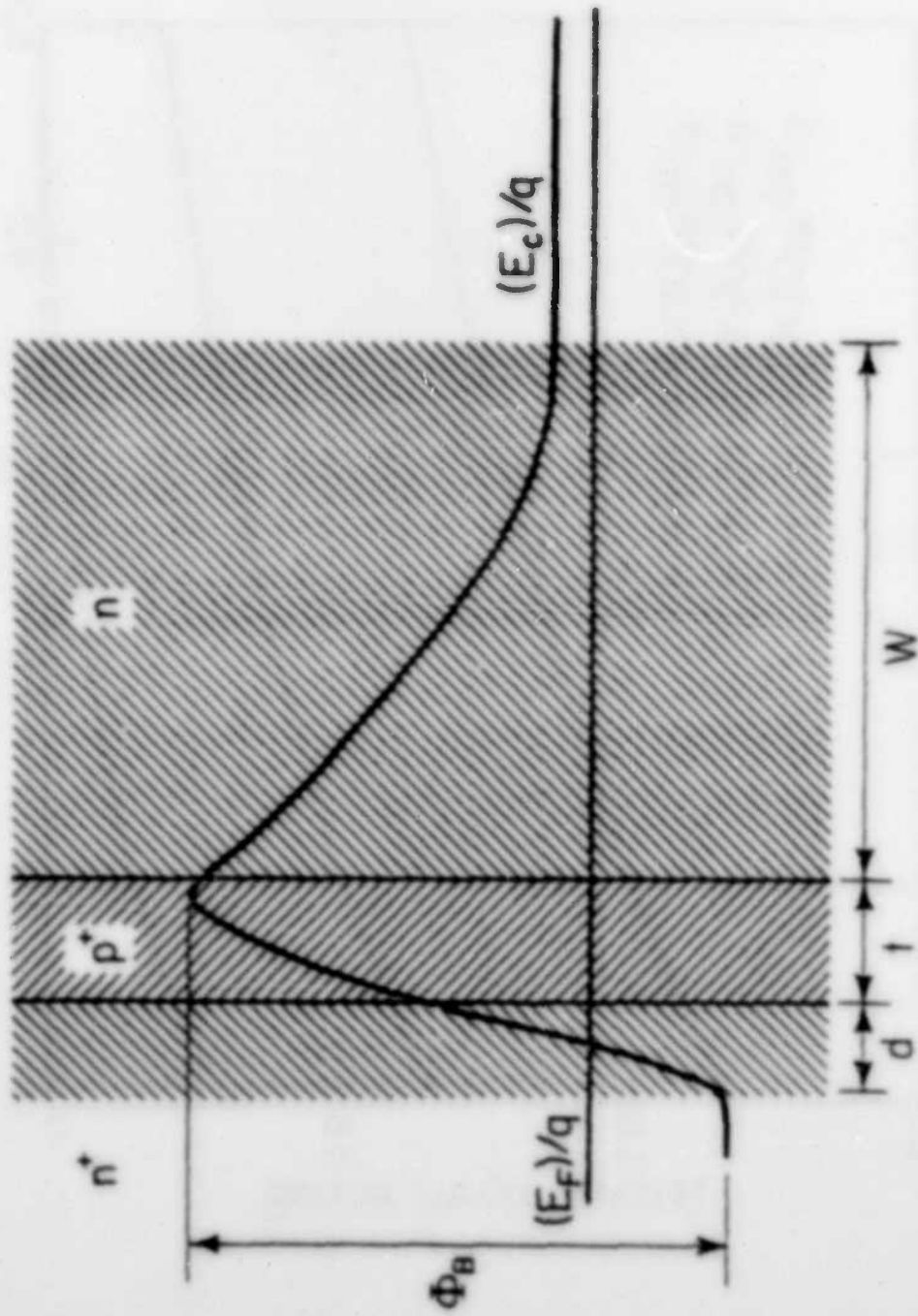


Fig. A2



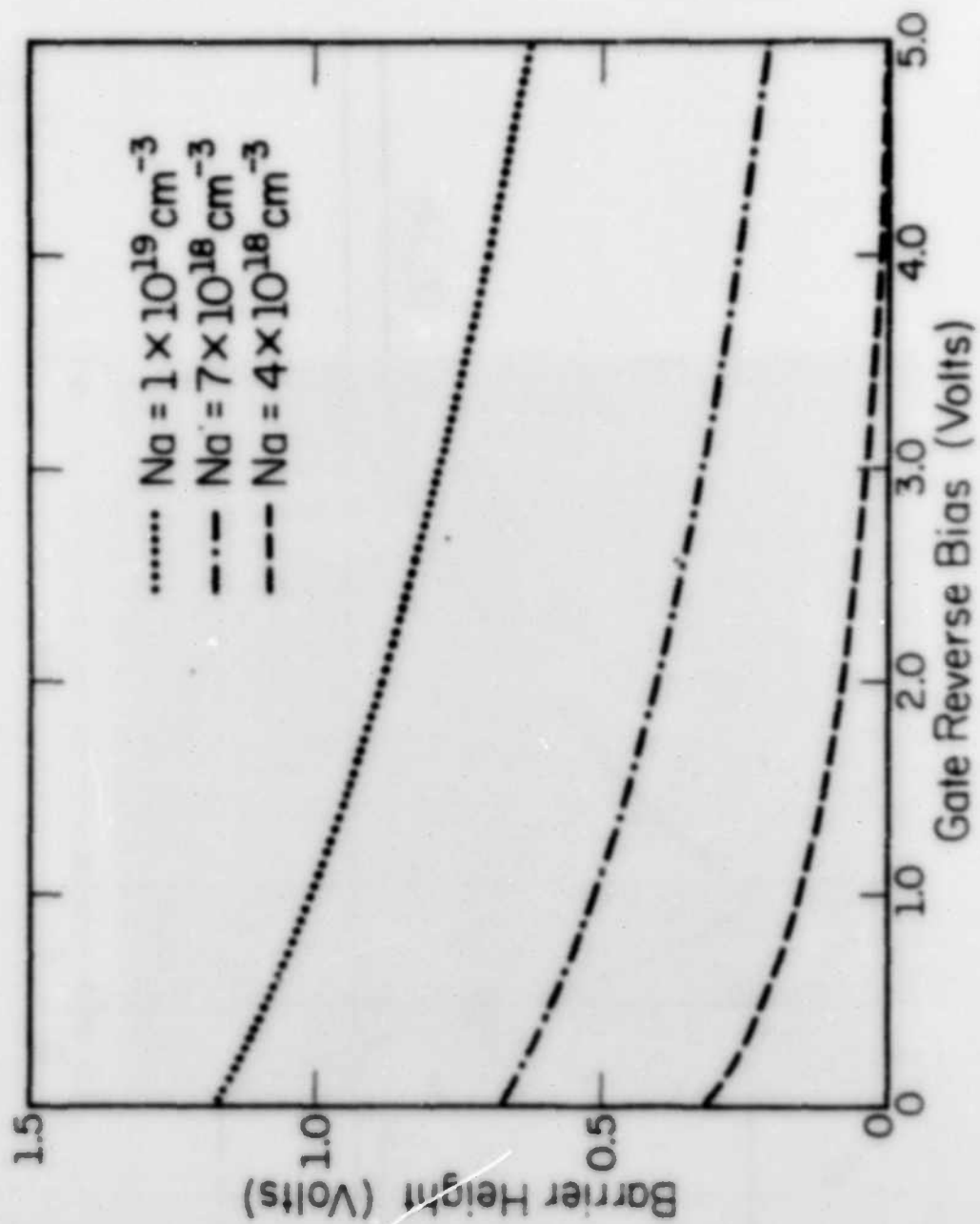
YP-266

Fig. 81

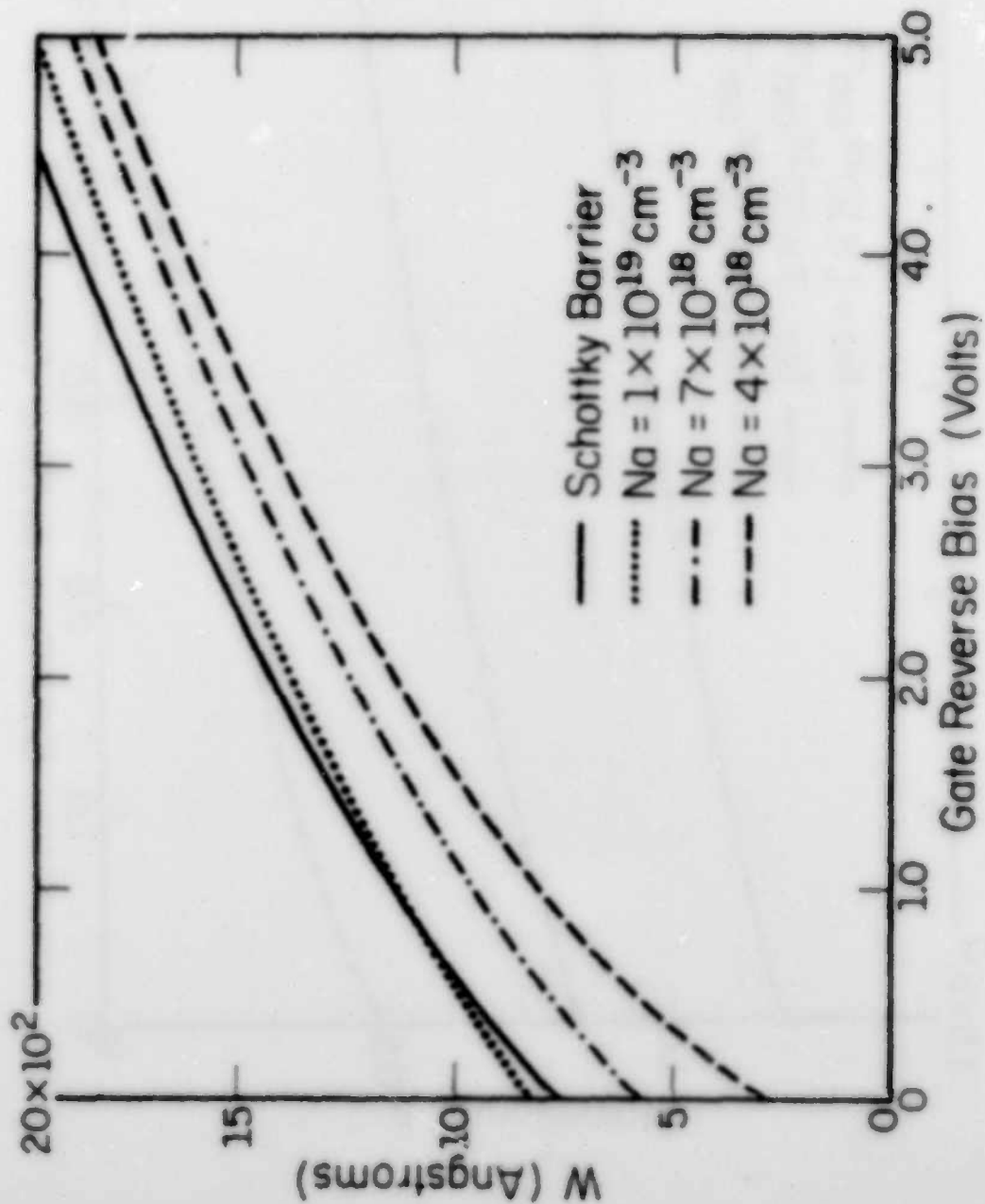


VP-224

FIG. 82

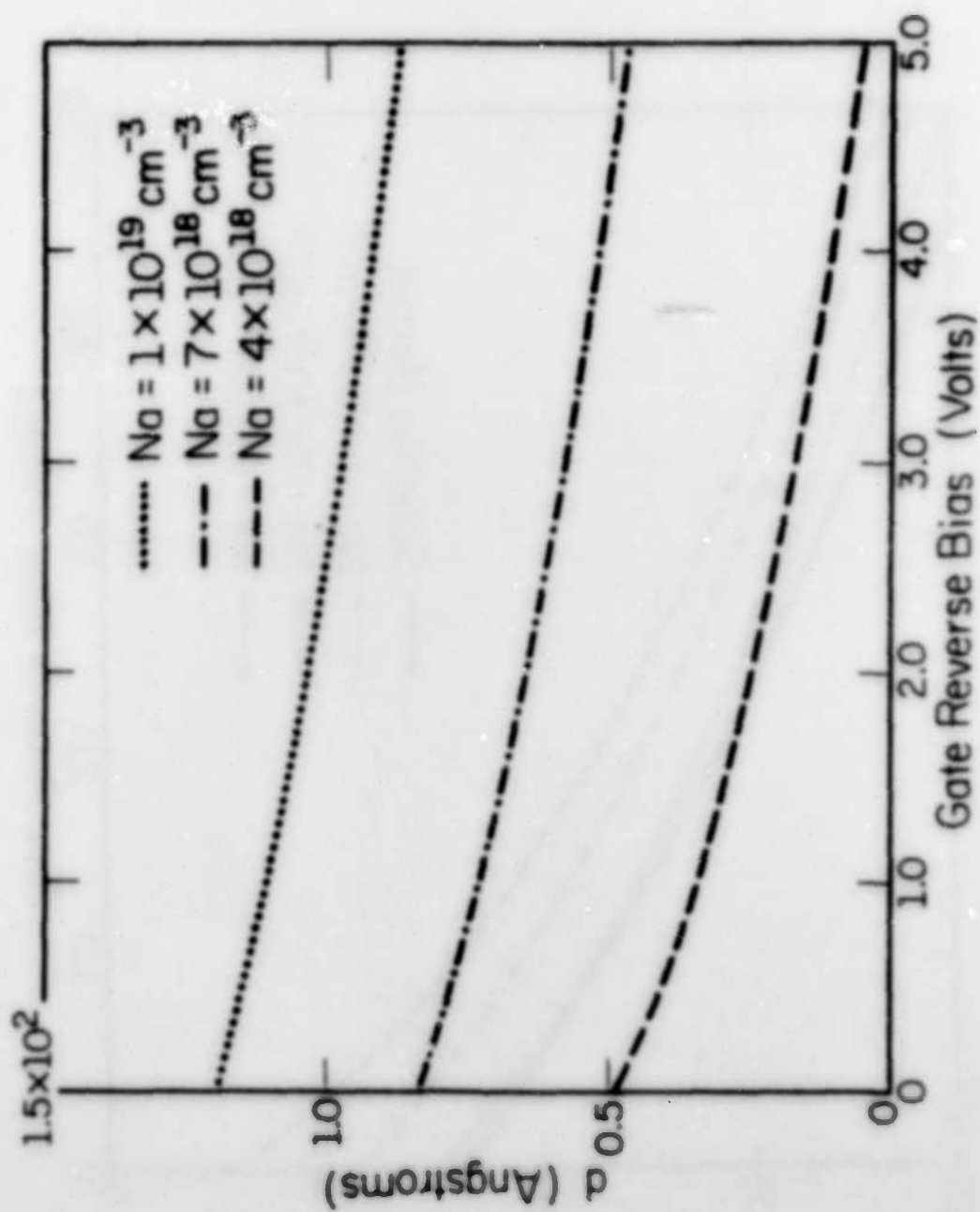


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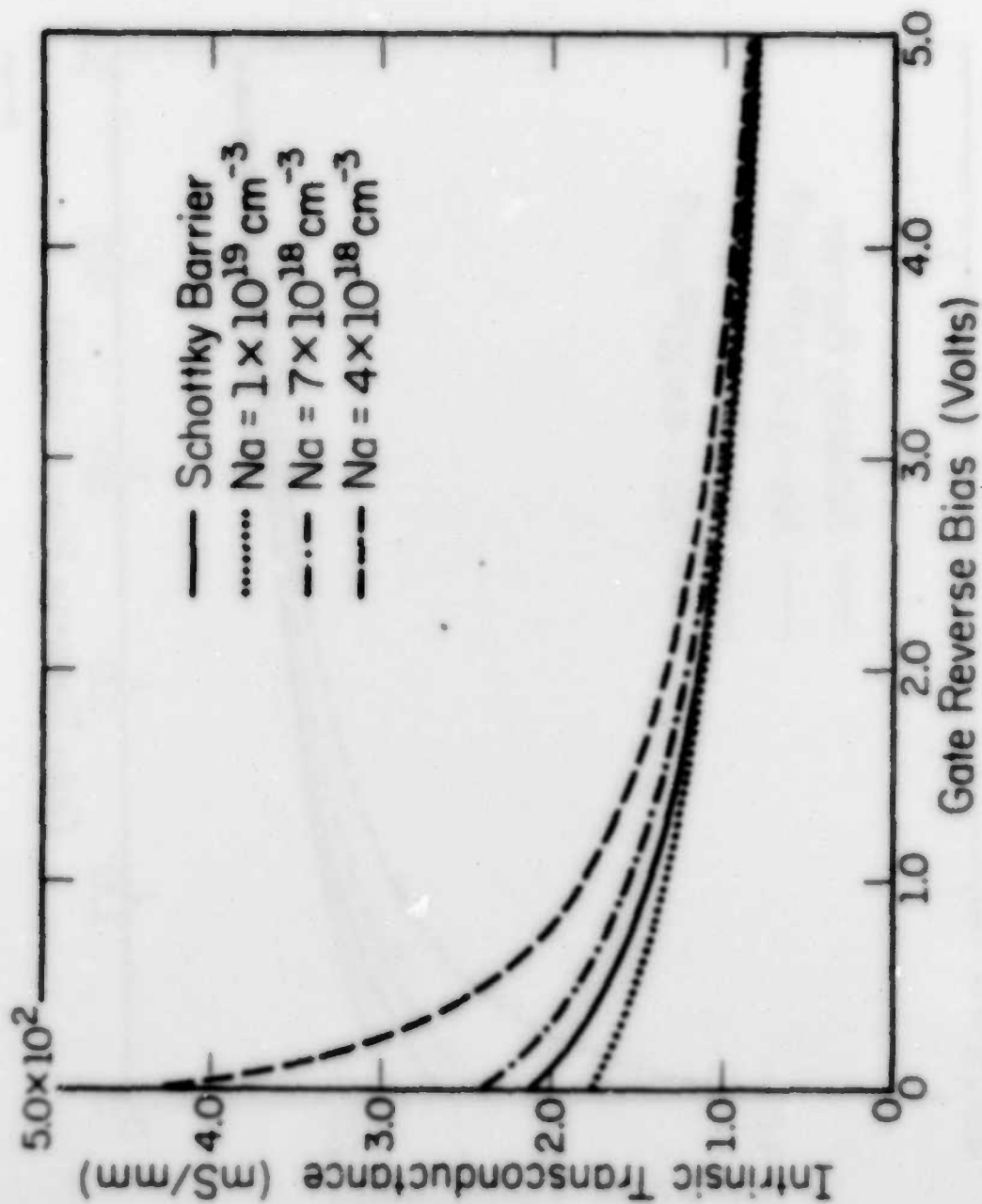
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Fig. 8A



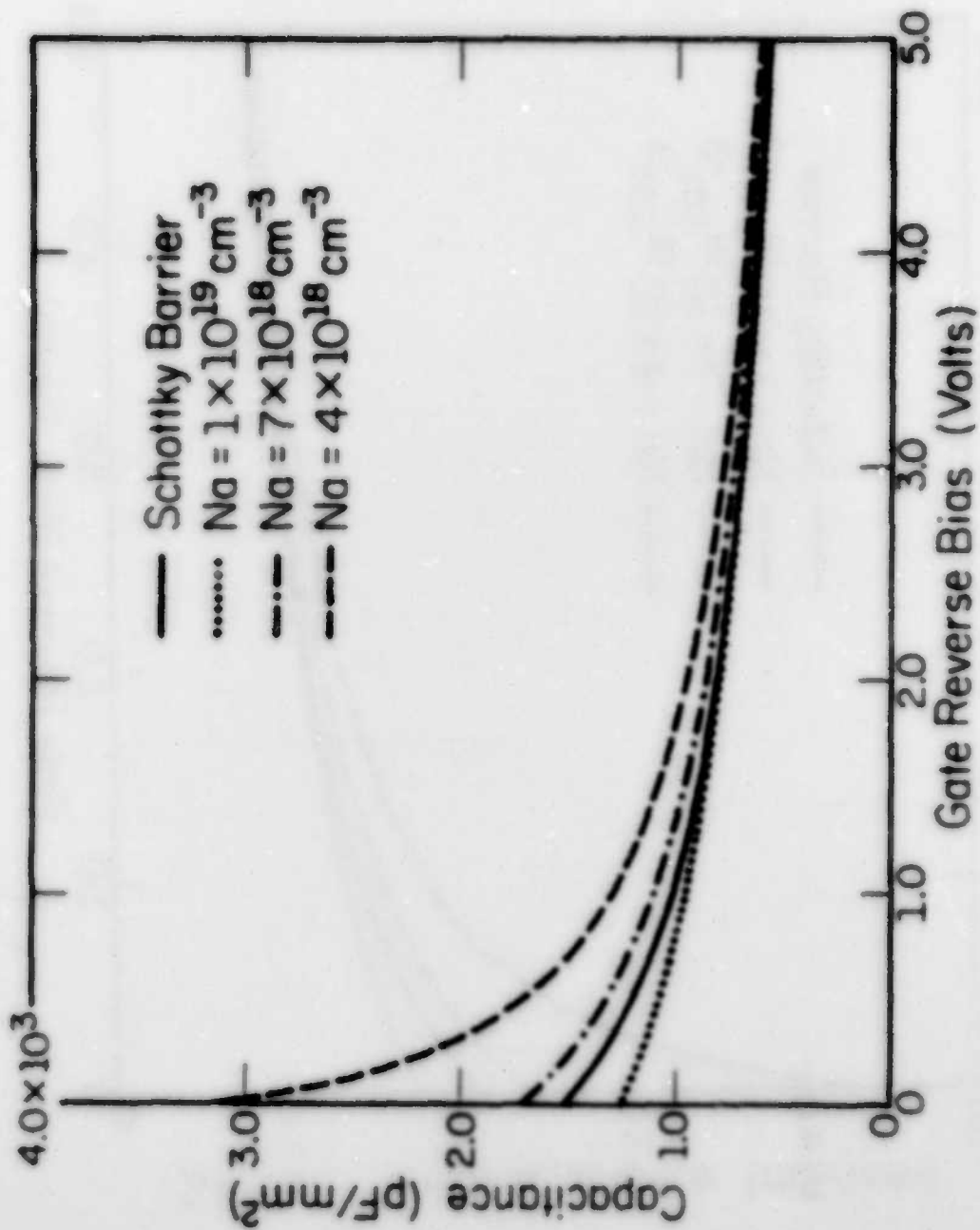
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Fig. 85



VP-219

Fig. 86



VP-220

Fig. B7

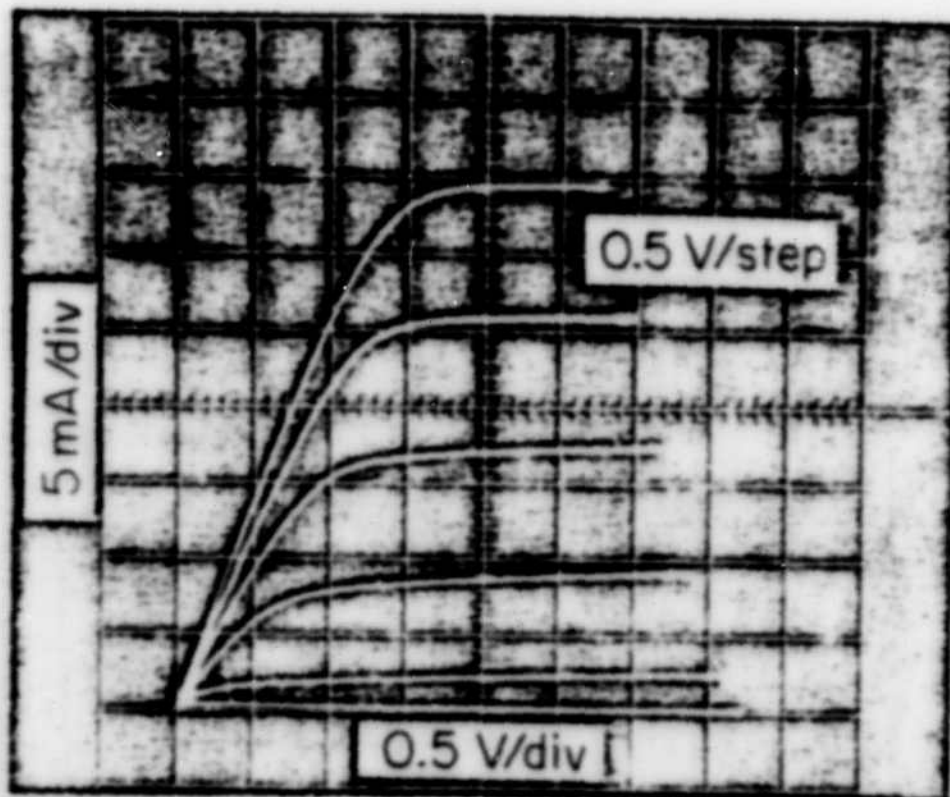


Fig. 88

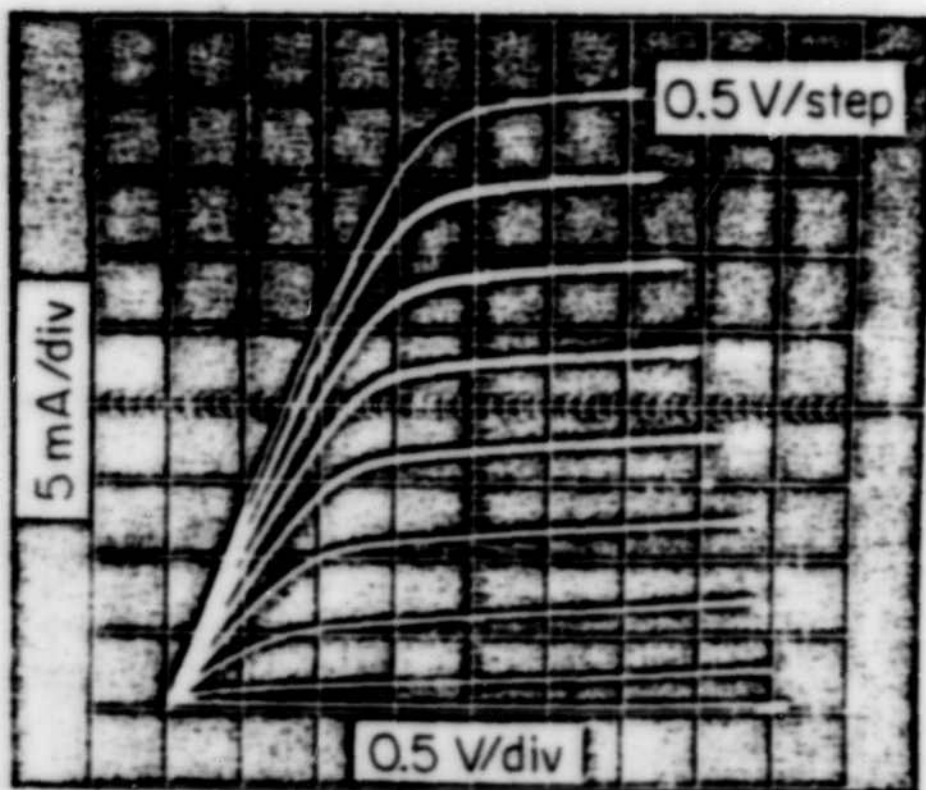
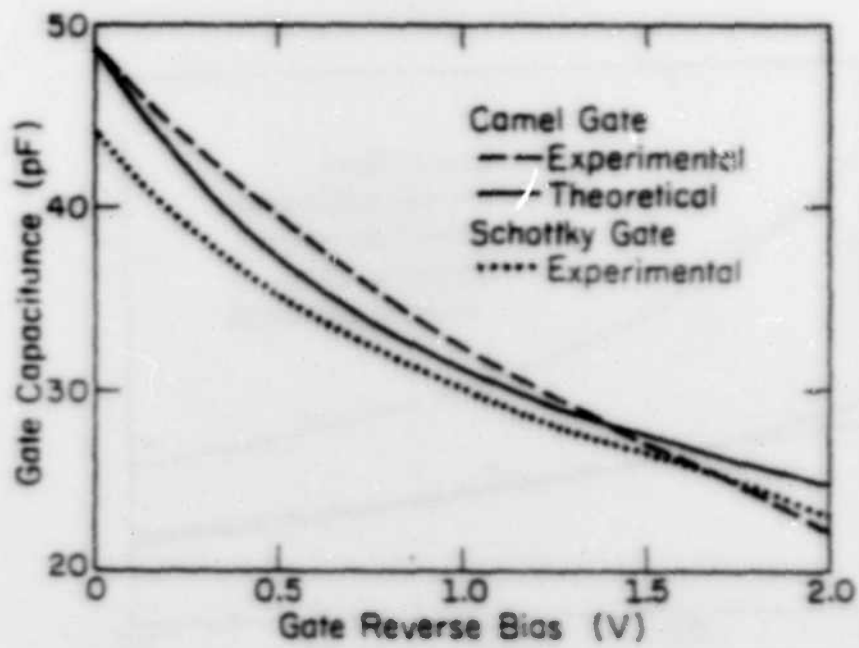
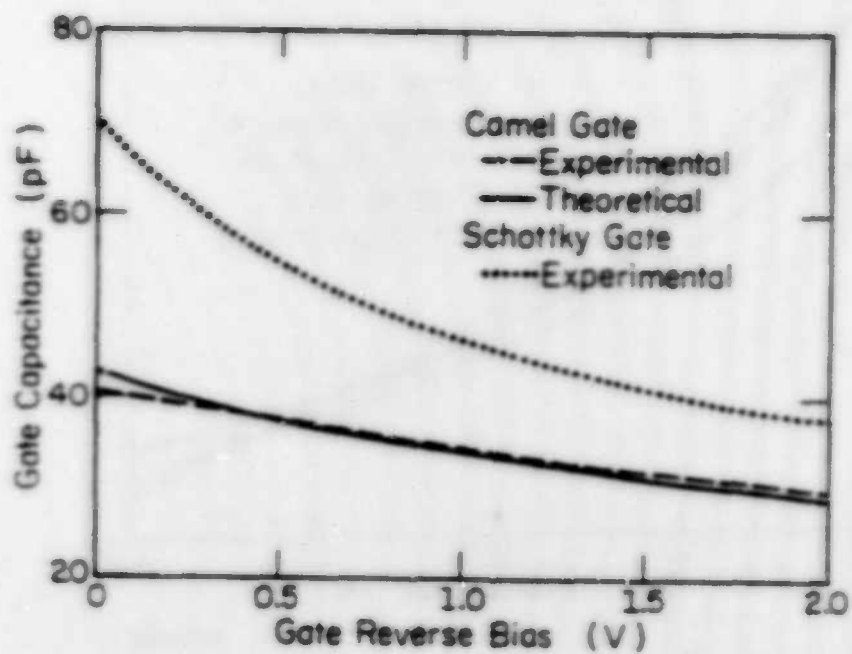


Fig. 89



YP-222

Fig. 810



YP-223

Fig. B11

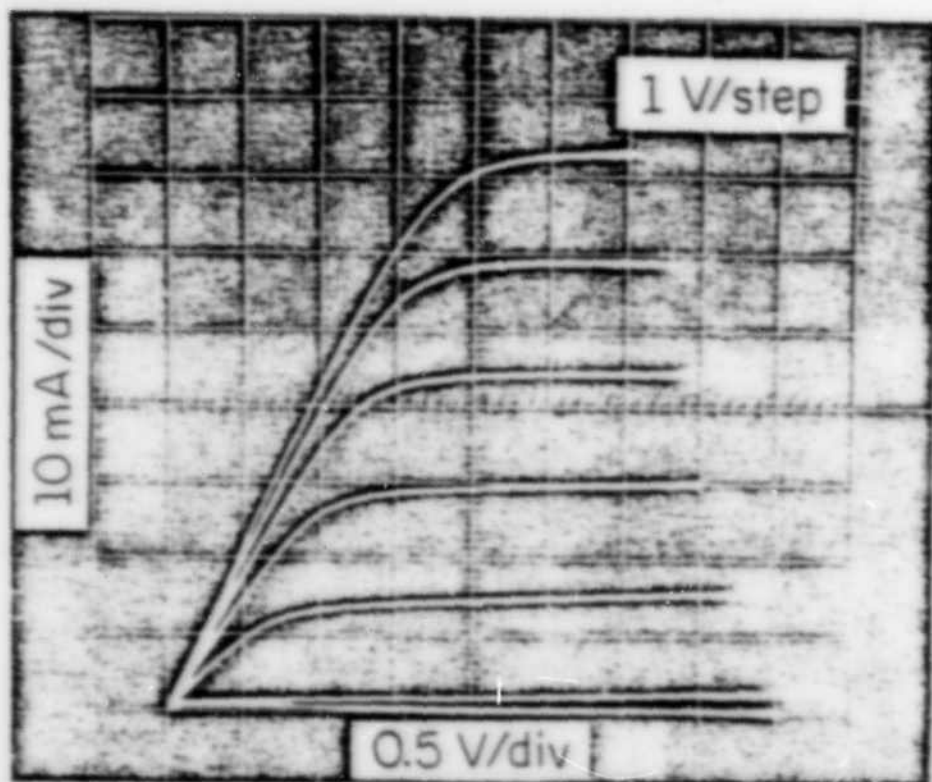


Fig. 812

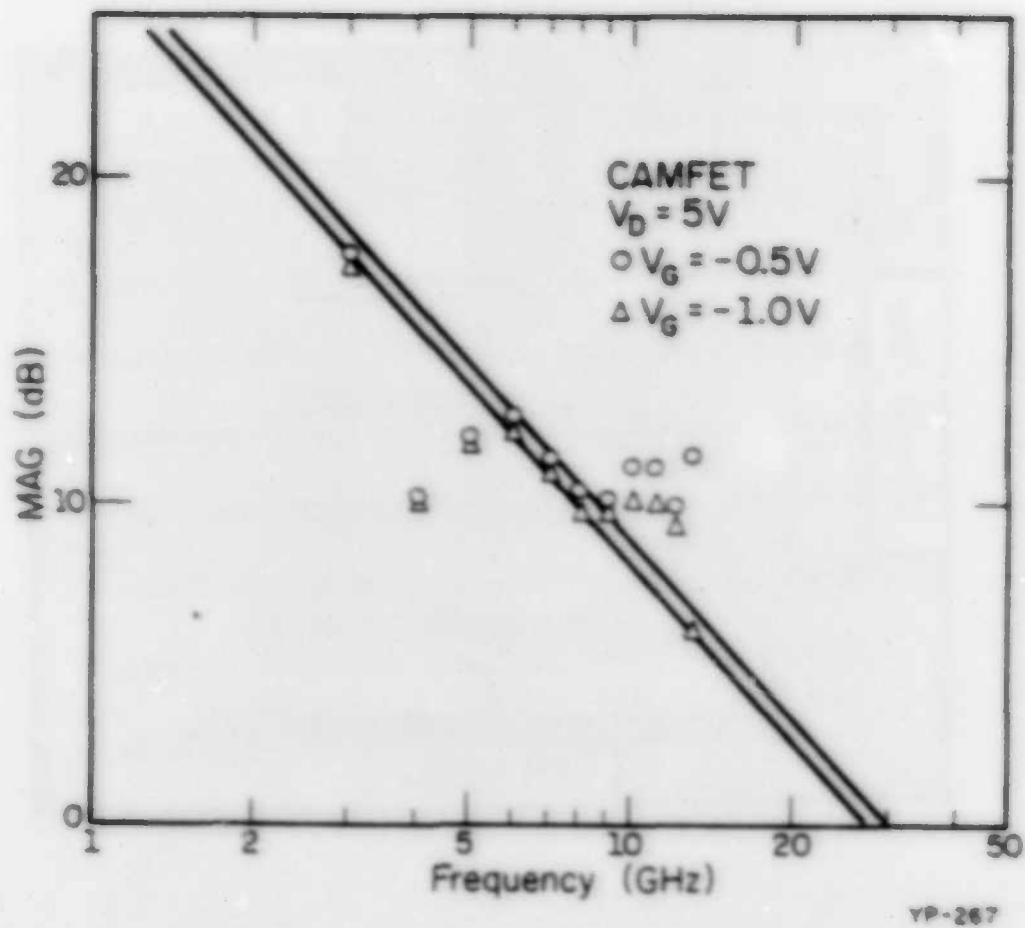


Fig. B13

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